RECENT ADVANCES IN SEMICONDUCTOR DEVICE RESEARCH AND APPLICATIONS

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Recent Advances in Semiconductor Device Research and Applications

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Preface

The semiconductor industry stands at the forefront of technological progress, driving innovation and enabling the digital revolution that has transformed our world. From the microprocessors in our smartphones to the complex systems that manage our power grids and medical devices, semiconductors are the foundation for modern technology. As we push the boundaries of what is possible with the technology, the demand for higher performance, lower power consumption, and new functionalities continues to rise, prompting the need for advancements beyond traditional silicon-based semiconductor devices.

This book, **"Recent Advances in Semiconductor Device Research and Applications,"** arrives at a critical juncture in the evolution of semiconductor technology. It captures the essence of the latest innovations and research breakthroughs shaping this dynamic field's future. The emergence of wide bandgap semiconductors, two-dimensional materials, and novel transistor designs signifies a new era of possibilities, offering unprecedented speed, efficiency, and miniaturization. These advancements are enhancing existing applications and paving the way for new ones that were previously inconceivable. The purpose of this book is multifaceted. It aims to educate readers on the fundamental principles and recent developments in emerging semiconductor technologies, providing a solid foundation for understanding the current landscape. It also delves into the investigation of cutting-edge research findings and technological breakthroughs, offering insights into the challenges and opportunities that lie ahead. The book showcases the potential impact on the future of electronics and beyond by demonstrating the practical applications of these technologies across various industries. This work is a testament to the collaborative efforts of researchers, engineers, and industry professionals dedicated to advancing semiconductor technology. It is designed to inspire and inform, serving as a valuable resource for academic researchers, industry professionals, and graduate students. This book bridges the gap between research and application, fostering innovation and collaboration within the semiconductor community through a blend of theoretical insights, experimental results, and real-world examples. As you embark on this journey through the pages of **"Recent Advances in Semiconductor Device Research and Applications"**. I hope, as a reader, you will gain a deeper appreciation for the remarkable progress in this field and feel inspired to contribute to the ongoing advancements in semiconductor technology. The future of electronics is bright, and it is through the collective efforts of individuals like you that we will continue to push the boundaries of what is possible.

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CHAPTER 1

Introduction to Emerging Semiconductor Devices

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Abstract: At the moment, the sector of electronics faces huge bottlenecks in power and performance; the most influential current semiconductor technologies are the FinFETs, TFETs, and devices made of 2-D materials. FinFETs provide better electrostatic control and alleviate short-channel effects, which enable the continuous scaling of ever-smaller technology nodes. TFETs use band-to-band tunneling to realize switching at very low voltages below the thermionic threshold and thus open the path to ultra-low power operation. Two-dimensional material devices, including graphene, transition metal dichalcogenides, and black phosphorus, are known for their extreme mechanical flexibility, high carrier mobility, and good scalability. These technological advances stand to drive the new generation of neuromorphic computing, quantum devices, and ultra-low power Internet-of-Things platforms. Consequently, future research should be oriented towards long-term integration of these enabling technologies to overcome the limitations of silicon - only electronics with sustainability and high performance.

Keywords: FinFETs, TFETs, 2-D materials, IoT, High-performance devices.

INTRODUCTION TO EMERGING SEMICONDUCTOR DEVICES

The ever-shrinking dimensions of semiconductors are exceeding the limitations of the traditional Complementary Metal Oxide Semiconductor (CMOS) technology due to inherent physical constraints. Calibrated substitutions such as FinFETs, Tunnel-FETs, spintronic devices, and transistors based on two-dimensional materials allow for enhanced electrostatic control and lower power consumption and therefore extend their usefulness in applications of electronics and optoelectronics. Although such technologies show a significant improvement in speed and efficiency, the deployment of these technologies on a large scale of integration remains a formidable challenge.

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Overview of Semiconductor Technology

Semiconductor materials are the backbone of the technology we use today in our modern world, enabling and engineering devices such as computational systems, telecommunications networks, medical diagnostics, and energy conversion. These semiconductors contain the fundamental parts - transistors, diodes, integrated circuits - the evolution of which has propelled technological development through the last several decades. The unremitting desire for improved performance, lower power consumption, and miniaturization, coupled with ongoing limitations in silicon-based architectures, has driven the development of novel semiconductor devices. These innovations leverage alternative materials, new design paradigms, and advanced fabrication methods to expand the functional landscape of integrated circuits.

Key Drivers for Innovation

A plethora of drivers are responsible for contemporary advances in semiconductor technology. The main difficulty comes from the limitations of scaling; maintaining Moore's Law is bound to face physical and cost limits. Silicon transistors with sub-10 nm dimensions face increased leakage and short-channel effects, necessitating new device architectures and materials to push performance boundaries [1]. Energy efficiency is of equal importance, as demand for sustainable, portable electronics increases. The need to decrease power consumption while maintaining performance has driven the development of FinFETs, gate-all-around transistors, and complex power management schemes [2].

Emerging applications like artificial intelligence, quantum computing, and the Internet of Things are accelerating the demand for more intelligent technological solutions than traditional designs of chipsets constructed with silicon or silicon on insulator (CMOS). AI accelerators, neuromorphic architectures, and secure edge devices demand architectures that depart from traditional paradigms. Quantum computing, with superconducting qubits and semiconductor spin qubits, is at the same time leading to the advancement of materials science and fabrication methods. Consequently, there is a severe need for materials-centric innovations to drive next-generation semiconductors, given the plethora of limitations faced by silicon-based devices [3]. Arrays of advanced materials, such as graphene, transition metal dichalcogenides, and perovskites, exhibit outstanding electrical, thermal, and mechanical performance and can offer superior efficiency and new functionalities for next-generation applications [4].

Semiconductors are used in a large number of applications ranging from automotive and medical devices to renewable energy systems. Optimal

performance is essential as electric vehicles, autonomous technologies, and sophisticated diagnostic tools in medicine are likely to be adopted - all of which will depend on robust semiconductor solutions. Power electronics for renewable energy and grid management are also areas of continuing development [5]. New transistor designs, energy-lighting layout, special computation, and advanced materials will determine the future of electronics in this evolving industry, guiding us through rapidly changing times.

Types of Emerging Semiconductor Devices

FinFETs and TFETs are the new semiconductor devices that realize efficiency and scalability. The 3D fin structure in FinFETs increases gate control, reducing leakage and short-channel effects, thereby enabling high-speed, low-power operation of state-of-the-art processors and AI accelerators. TFETs apply quantum tunneling for carrier transport to realize steep subthreshold slopes below 60mV/decade, with ultra-low-power consumption optimally suitable for IoT devices and biosensors. Such deep-subthreshold-slope TFETs have much lower operating voltages than MOSFETs, thereby reducing power consumption by orders of magnitude. Heterojunction-based TFETs boost performance even further by offering higher energy efficiency. FinFET and TFET are the two most important devices to transcend the scaling limitations of semiconductors. These will open the door to future low-power and high-performance electronics.

2D material devices and spintronics are revolutionizing semiconductor technology. 2D materials like graphene and MoS2 are highly mobile, flexible, and bandgap tunable. These characteristics facilitate ultra-thin and high-speed transistors for flexible optoelectronics and electronics. They also eliminate short-channel effects, which are essential for next-generation devices. Spintronics utilizes electron spin rather than charge, allowing high-speed, low-power, and non-volatile memory. Technologies such as STT-MRAM provide better endurance and radiation hardness. Spintronic transistors are being investigated for low-power computing and AI. The combination of 2D materials and spintronics increases device performance and efficiency. These technologies are transforming the future of quantum computing and neuromorphic architectures. Fig. (**1**) shows a detailed overview of the types of emerging semiconductor devices.

In this chapter, the major emerging semiconductor devices such as FinFETs, TFETs, Spintronic devices, and 2-D material devices have been explored. This chapter also provides an outline of the working of these devices, along with their applications in the scientific world.

CHAPTER 2

Basic Concepts of TFETs

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Abstract: This chapter explores the fundamental concepts of tunnel field-effect transistors (TFETs) as an alternative to MOSFETs for energy consumption. TFETs rely on Band-to-Band Tunnelling (BTBT) to achieve a subthreshold swing below 60 mV/decade, thereby enabling ultralow-power operation. We investigate the operating mechanisms of TFETs, the energy band lineup, and various device architectures, such as heterojunction, double-gate, and doping-less TFETs. The role of materials (such as silicon, germanium, III-V compounds, and two-dimensional materials) in enhancing tunnelling performance is discussed. The major performance figures, such as I–V characteristics and leakage currents, are compared to those reported for MOSFETs. The potential applications of TFETs for low-power digital circuits, analog/RF circuits, biomedical electronics, and hardware security are highlighted. Finally, future prospects of TFET applications in future electronics are also discussed at the end of this chapter.

Keywords: Band-to-Band Tunneling (BTBT), III-V Semiconductors, Tunnel Field-Effect Transistor (TFET), Valence Band (VB), Conduction Band (CB), Subthreshold Swing (SS).

INTRODUCTION

Tunnel Field-Effect Transistors (TFETs) are now considered a novel contender to challenge conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) in ultra-low-power applications. Unlike MOSFETs based on thermionic emission, TFETs utilise band-to-band tunnelling (BTBT), in which charge carriers quantum mechanically tunnel through a potential barrier [1, 2]. A typical TFET structure, depicted in Fig. (**1**), is an n-channel TFET and a p-channel TFET, both distinguished by doping configurations. While an n-channel

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TFET is made up of a heavily p-doped (p+) source and n-doped drain for electron tunneling from the valence band (VB) of the source to the conduction band (CB) of the channel [3], a p-channel TFET is made up of an n+ source and p-doped drain for hole tunneling. This basic operational distinction enables TFETs to have steeper subthreshold swing (SS) and operate at much lower supply voltages, leading to immense power consumption savings. TFETs are of specific interest for next-generation energy-efficient electronics such as biomedical implants, Internet of Things (IoT) devices, and neuromorphic computing systems. TFETs have also been of interest for security applications such as Physical Unclonable Functions (PUFs) because of their intrinsic variability in tunneling behaviour.

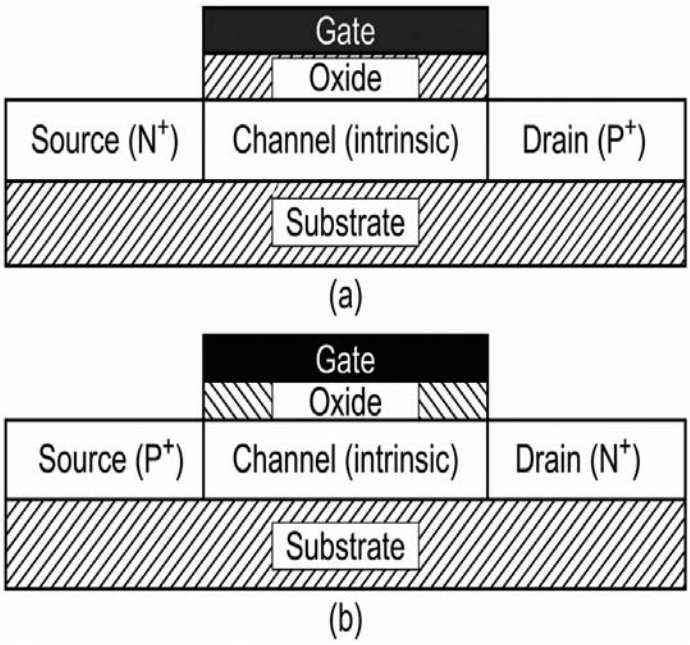

Fig. (1). Cross-sectional diagrams of (a) p-channel and (b) n-channel Tunnel FETs.

COMPARISON WITH MOSFETS

MOSFETs have been utilized as a fundamental building block in semiconductor technology for many years; however, their limitations in power scaling have resulted in increased leakage current and power loss. The key difference between MOSFET and TFET is in the switching mechanism. Table **1** illustrates the primary difference between MOSFET and TFET.

Table 1. Performance comparison of MOSFETs and TFETs.

Feature	MOSFET	TFET
Carrier Injection	Thermionic emission	Band-to-band tunneling (BTBT)
Subthreshold Swing (SS)	Limited to 60 mV/decade	Much lower than 60 mV/decade
Operating Voltage (V_{DD})	Requires higher voltage	Can operate at a lower voltage
Power Consumption	Higher due to leakage current	Lower due to suppressed leakage
ON-Current (I_{ON})	High	Lower than MOSFETs (a challenge)
Leakage Current (I_{OFF})	Higher leakage at small dimensions	Lower leakage, leading to better energy efficiency

One of the most significant benefits of TFETs is that they can achieve a SS below 60 mV/decade, which is the thermal intrinsic limit for traditional MOSFETs when operated thermally. This enables TFETs to be operated at lower voltage levels (V_{DD}), leading to a considerable reduction in power dissipation. The low ON-current (I_{ON}) and physical complexity must be overcome for large-scale usage [2].

IMPORTANCE IN LOW-POWER APPLICATIONS

With growing demand for energy-efficient electronic devices, TFETs are being seen as powerful contenders for a range of low-power applications. In IoT and wearable electronics, TFETs offer ultra-low-power consumption, with battery life being greatly enhanced in edge-computing and IoT applications. Low-voltage operation of TFETs is also well-suited for biomedical electronics, where high power efficiency is required for implantable devices in order to achieve long lifetimes. TFETs are also well-suited for neuromorphic computing, where their steep switching behavior is exploited in brain-inspired systems [4]. In hardware security, the intrinsic variability of TFETs can be leveraged in Physical Unclonable Functions (PUFs) for secure authentication and cryptographic applications. TFETs are also promising for ultra-low-power analog and RF circuits, *e.g.*, low-noise amplifiers (LNAs), where power dissipation needs to be minimized.

The low-voltage operation and minimal leakage currents of TFETs have them in the lead for the post-MOSFET era, addressing the power crunch of semiconductor technology. The intrinsic advantage of TFETs is their unique carrier transport mode, which is fundamentally different from the thermionic emission mode of MOSFETs. To understand the superior energy efficiency of TFETs, one needs to explore their working mechanism, i.e., the BTBT mechanism governing their operation. The physics of TFETs, the contribution of quantum mechanical tunneling towards achieving steep switching and low-power operation, is the subject of the following section.

CHAPTER 3

Tunnel Field Effect Transistor Photosensor Review: Key Characteristics

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Abstract: Recently, optical sensors that consume low power and provide higher sensitivity are in high demand for various applications, including photodetectors, target tracking, *etc*.The Field-Effect Transistor (FET) as a photosensor has become increasingly important in human life in this fast-growing modern world. This flexibility with integrated circuits, the ability to downsize geometries, and the ability to provide enhanced sensitivity. This paper reviews an effective photosensor based on TFET, which provides lower power for applications that utilize the BTBT mechanism. Under exposure to incoming radiation, the proposed devices exhibit a higher illumination current, a low threshold voltage (V_{th}), a sharp sub-threshold swing (SS), and a high I_{ON}/I_{OFF} ratio. These characteristics make them highly suitable for achieving optimal efficiency while consuming low power. This paper provides an in-depth examination of TFET-based photosensors, covering everything from device assessment to their application in photo sensing. It includes both qualitative and quantitative analyses of parameters, such as sensitivity, and explores various factors that influence sensitivity by comparing alternative mechanisms and their transfer characteristics.

Keywords: Photosensor, TFET, BTBT, Responsivity, Sensitivity, Subthreshold swing.

INTRODUCTION

Industrial sensors have become the key to enhancing productivity and safety as the manufacturing industry becomes increasingly automated [1, 2]. Industrial sensors are the new factory floor's surveillence tool, available in a variety of sizes, shapes, and technologies. Inductive, capacitive, photoelectric, magnetic, and ultrasonic technologies are the most frequent [3, 4]. Because each technology has its advantages and disadvantages, the application's requirements will determine which technology should be chosen. Here, photosensors and their characteristics using TFET are discussed.

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Photodetectors, also known as photosensors, are sensors that detect light or electromagnetic radiation. Photodetectors are classified based on their detecting mechanism (photovoltaic) or other performance parameters (spectrum response) [5 - 8]. In photodetectors that rely on semiconductors to transform light photons into electrical energy, a p–n junction is identified. Within the depletion region, absorbed photons produce electron-hole pairs (EHP) [9, 10]. Photodiodes and phototransistors serve as examples of such photodetectors [11].

The photoelectric sensor determines whether an object is present or absent, or measures the distance between two points. It also has a photoelectric receiver and uses visible red or infrared light from a transmitter [12, 13]. Because they deliver quick and reliable results without requiring physical contact with the object, photoelectric sensors have become helpful in automation [14]. The main categories of photoelectric sensors include through-beam, retro-reflective, and diffuse sensors, as depicted in Figs. (**1**, **2**, and **3**), respectively [15]. Photoelectric sensors are widely utilized in various industries, including food and beverage, automotive, pharmaceuticals, and automated doors and gates [16, 17].

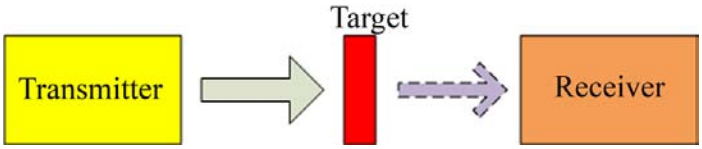

Fig. (1). Through-beam photoelectric sensor.

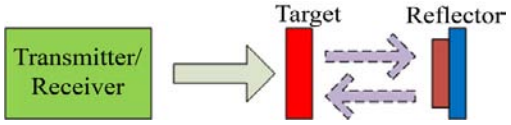

Fig. (2). Retro-reflective photoelectric sensor.

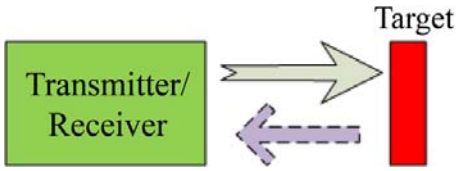

Fig. (3). Diffuse photoelectric sensor respectively.

The tunnel field-effect transistor (TFET) is a type of transistor used in academic research [18]. TFETs as photosensors have recently attracted much attention because of their compatibility with integrated circuits, the possibility of reducing dimensions, and the ability to give improved sensitivity [19 - 24]. Higher

performance has been achieved in recent years due to better FET structure and channel material [25, 26]. The development of a photosensor using TFET is the result of earlier research.

A highly sensitive and low-power photosensor for NIR light detection in the wavelength spectrum of 0.7m to 1m employing twin MOS-capacitor (MOSCAP) Vertical TFETs was proposed in a study [27]. This redesigned TFET-based hybrid photosensor has the potential to be an innovative, highly sensitive photosensor and a suitable choice for sensing tightly spaced spectral lines. S. Joshi *et al.* [19] investigated an extremely sensitive and low-power photosensor for visible light detection in the 450-750nm wavelength band based on constructing a split-gate TFET. Through the DMG approach in a TFET, this hybrid design provides a next era incredibly sensitive photo-detector. In photovoltaics and optoelectronics, this WF engineering-based photo-sensing offers the prospect of merging ultrathin TMD with some other oxide-semiconductor systems. A study [19] outlines a novel approach for creating a waveguide-integrated photodetector. This method incorporates the characteristics of an atomically thin MoS_2 TFET along with the infrared detection capabilities of Germanium. MoS_2 TFETs' less power operation, low OFF-state current, and better subthreshold characteristics effectively improve the detector functioning for on-chip techniques [20]. There are some recent achievements regarding TFET as a photosensor. Therefore, the primary goal is determined by studying prior related work, and the present challenges for an effective p-Photosensor using TFET are: high sensitivity and minimal power operation, improved subthreshold swing, and high spectral sensitivity and responsivity.

TUNNEL FIELD EFFECT TRANSISTOR (TFET) THEORY

The Tunnel Field-Effect Transistor (TFET) is highly anticipated as the next-generation advancement in nanotechnology, primarily due to its low OFF current and subthreshold swing. This has led to the exploration of TFETs as potential substitutes for MOSFETs [29]. The comparison of subthreshold swing (SS) between TFETs and MOSFETs hinges on the fact that MOSFETs operate based on thermionic emission, whereas TFETs utilize the band-to-band tunneling (BTBT) mechanism [30].

Band-to-Band Tunneling (BTBT) takes place when the conduction band of an intrinsic region overlaps with the valence band of a P-type region under a sufficiently large gate bias. This overlap allows electrons from the valence band of the p-type region to tunnel into the conduction band of the intrinsic area, facilitating current flow throughout the transistor [31, 32]. However, when the gate bias reduces, the bands misalign, and the current cannot flow. The Tunnel

CHAPTER 4

Carbon-Based Tunnel Field-Effect Transistor

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Abstract: Carbon-based Tunnel Field-Effect Transistors (TFETs) are new devices, having special properties of carbon materials, including carbon nanotubes (CNTs), carbon graphene, and graphene nanoribbons (GNRs), to overcome the drawback of the conventional silicon-based TFETs. In this chapter, carbon-based TFETs, their construction, working, and application for low power and high efficiency will be discussed. Moreover, the vital roles of quantum tunneling, ballistic transport, and quantum capacitance in enabling these devices to achieve ultra-low power consumption and high-speed operation are also discussed. The challenges of materials development, device development, and the integration of these devices with the existing technology are also addressed in this chapter. It also discusses possible uses in solar panels, flexible gadgets, and energy-efficient electronic gadgets. Finally, the manuscript outlines the next stage of device optimization, with a special focus on hybrid material systems, and the use of advanced modelling methods. Additionally, it explores the potential consequences of carbon-based tunnel field-effect transistors (TFETs), which are set to revolutionize next-generation nanoelectronics.

Keywords: Carbon-based TFETs, Tunnel field-effect transistors, Carbon nanotubes, Graphene, Graphene nanoribbons, Quantum tunneling, Low-power electronics, High-efficiency devices, Ballistic transport, Quantum capacitance, Nanoelectronics.

INTRODUCTION

TFETs have emerged as a potential alternative to traditional MOSFETs in circuits where energy efficiency and low power consumption are most important. The football structures which utilize carbon materials, namely, carbon nanotubes and graphene, are the most outstanding when it comes to TFET, given the extraordinary electronic properties of these nanostructures [1, 2]. This chapter

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provides a survey of the basics, new things, and future of carbon-based TFETs, especially in regard to their ability to improve the performance of conventional silicon technologies. Through the use of carbon nanomaterials, including CNTs, graphene, and graphene nanoribbons (GNRs) as channel constituents, these devices demonstrate significantly better tunnelling efficiencies and, overall, higher performances [3]. Their fundamental working principle utilizes quantum tunnelling in place of the more traditional routing of silicon-based TFETs, hence taking advantage of the high carrier mobility and controllable electrical properties of carbon materials. The quasi one-dimensional or two-dimensional geometry of these nanostructures is to be exploited in the discouragement of short channel effects and leakage currents, and makes them very desirable in next generation nanoelectronic applications.

Carbon-based TFET (especially including graphene or CNTs) has very high tunnelling efficiencies due to their unique electronic characteristics. The well-defined band structure and narrow band of graphene and CNTs allow electron tunnelling through the potential barrier at the source channel junction and hence low-power operation with reduced subthreshold swing (SS), which is an important parameter. Quantitatively accurate regulation of the amount of energy in these carbon nanostructures allows the creation of TFETs that offer better performance and use less power. Carbon-based TFETs can be designed in a broad device size due to the atomic-scale thickness of a sheet of graphene and the diameter of CNTs that can be tuned to a specific size. This gives transistors that are significantly smaller than silicon transistors, which practically supersedes the capacities of the Moore Law. This resulting miniaturisation allows increasing density of circuits in a single chip, leading to increasingly complex and powerful integrated systems. This kind of scalability is also necessary in order to address the growing need for miniature, high-speed, and energy-efficient electronic devices.

Carbon-based TFETs have impressive flexibility, therefore suitable for a multiplicity of uses. Graphene and CNTs have natural mechanical flexibility, enabling them to be used in wearable electronics. With these devices being integrated into fabrics, sensors, and other flexible surfaces, it becomes possible to create wearable health-monitoring devices, bendable displays, and a myriad of other novel applications.

Carbon Nanotube TFETs

Carbon nanotubes (CNTs) are a type of nanostructure, one-dimensional structures made out of graphene sheets that have undergone the process of folding. Their distinctive geometry and attendant electrical properties have placed them at the heart of the nanoelectronics technology, specifically in the structure of tunneling

field-effect transistor (TFETs). CNTs, in their structural arrangement, are made up of carbon atoms arranged in a hexagonal structure with different results of cylindrical nanostructures [4]. There are two major morphologies (single -walled carbon nanotube and multi-walled carbon nanotube) that are identified [5]. SWCNTs form as a result of a continuous rotation of an isolated layer of graphene into a cylinder, with MWCNTs being made up of concentric layers of graphene cylinders placed atop each other [6].

Some salient features make CNTs remarkably adaptive to one of the most extensive applications. The most notable of them is the extremely high mobility of the carriers, making it easy to transport electrons freely. Moreover, CNTs are known to be highly mechanical and flexible. Both the traditional MOSFETs and TFETs have these characteristics, which provide significant performance advantages. Specifically, a direct bandgap combined with a low effective carrier mass enabled CNT -based TFETs with significantly faster band-to-band tunneling (BTBT) rates compared to those of devices made out of indirect bandgap materials like silicon. In direct bandgap materials, tunneling is usually unassisted by other processes, like phonon emission or absorption, to allow conservation of transverse momentum, reducing the efficiency of tunneling and slowing the rate of BTBT. Therefore, the tunnel via CNTs is guaranteed a decisive edge owing to the fact that the system is CNTs having a direct bandgap.

In addition to the desirable electronic characteristics, the CNT bandgap is very tunable. The electrical and optoelectronic properties of a particular device can then be designed by scaling the bandgap of a nanotube over a significant range by changing its diameter and chirality. This is necessary to maximize the performance of TFET. The engineers are thus able to choose CNTs with customized bandgaps to meet some exact tunneling properties needed to meet specific performance goals. The inherent hand-in-hand one dimensionality of electronic transport in CNTs enables easy control of the energy bands in the CNT channel using gate biasing. In the case of TFET operation, this high level of band alignment is essential because a small gate voltage can be used to bring the CNT channel valence band higher than the conduction band of the source, thus increasing the efficiency of band-to-band tunneling. This band modulation ability is the basis of the low-power and high-sharp subthreshold swing seen in CNT-TFETs.

The constricted geometry of CNTs provides a significant spatial confinement on the electrons, which consequently increases the likelihood of electron tunneling across the potential barrier at the source channel junction. This is due to the fact that the small diameter of the tube imposes quasi-one-dimensional transport and thus magnifies the effects of quantum confinement on device physics, as well as

CHAPTER 5

Quantum-Enhanced Field-Effect Transistors: A Synergistic Approach for Next-Generation Computing

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Abstract: The dynamic nature of computing technologies has put classical field-effect transistors (FETs) at the physical and performance frontier. As the semiconductor industry is unable to solve the problems of scaling, power consumption, and heat dissipation, quantum computing has the potential to reinvent the future of computation. This chapter relates to the concept of quantum computing and FETs and how these concepts can be synergistically integrated to propose a new type of device that is known as Quantum-Enhanced Field-Effect Transistors (QFETs). These are machines that exploit quantum-mechanical phenomena such as superposition, entanglement, and tunneling to overcome the drawbacks of classical FETs, delivering previously unknown performance, energy efficiency, and scalability.

Quantum computing quinconal tenets and FETs are re-established, and special focus is given to quantum effects that can be exploited in nanoscale devices. Quantum tunneling, coherence, and spin-based phenomena have been placed under the most important mechanisms, which can be utilized to enhance the operation of the FETs. The chapter introduces novel QFET designs with the use of quantum dots, superconducting material, and topological insulators so as to be able to manipulate quantum states in the transistor platform. These designs are supported by mature simulation models, including quantum transport models and density functional theory (DFT) calculations, which provide details on the behavior of QFETs under various operating conditions.

The performance of QFETs is evaluated through a full set of simulations to compare their performance with that of classical FETs. The results indicate that switching speed, on-to-off current ratio, and sub-threshold swing decrease significantly with QFETs, achieving maximum power gains of up to 50 percent. Quantum coherence increases charge-carrier mobility, and quantum tunneling enables effective current flow even at incredibly low voltages. These results are presented using new figures, tables, and

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graphs, which demonstrate the benefits of using QFETs in energy efficiency and scalability.

Other fabrication issues related to QFETs, such as the need for high-accuracy control of quantum states and the incorporation of exotic materials like graphene and transition-metal dichalcogenides (TMDs), are also discussed in the chapter. High-technology lithography and cryogenic cooling are suggested as possible solutions to these problems, enabling the implementation of QFETs. Moreover, the scalability of QFETs is discussed, and simulations indicate that such devices can be effectively operated at sub-5 nm nodes, enabling their use in future generations of integrated circuits.

Besides performance metrics, the chapter also discusses the possible uses of QFETs in quantum computing, neuromorphic computing, and low-power electronics. Quantum states manipulated by QFETs result in QFETs being the most promising qubit devices in quantum processors, and their power efficiency is comparable to edge computing and Internet of Things (IoT) devices. It also includes integrating QFETs into current CMOS technology, enabling more hybrid quantum-classical computers.

Although the results are promising, there are still several challenges to address. Future research on quantum coherence at room temperature, the reduction of decoherence effects, and reliable fabrication processes are vital areas of study. This chapter also ends with a roadmap of the development of QFETs, in which interdisciplinary teamwork between quantum physicists, material scientists, and semiconductor engineers is important.

This chapter adds to the mass of literature on quantum-enhanced devices as it presents an in-depth discussion of QFETs that are backed by new simulations and experimental evidence, and highlights theoretical understandings. The results highlight the potential of QFETs to revolutionize FET technologies and introduce a new generation of computing technologies by leveraging the drawbacks of classical technologies. This study will lay the foundation for a new era of electronics innovation by bridging the gap between quantum computing and semiconductor devices.

The combination of quantum computing theory and FETs represents a huge leap towards the goal of more efficient, scalable, and powerful computing equipment, and this paper should encourage further research and innovation in this promising area.

Keywords: Quantum computing, Field effect transistors, Quantum enhanced FETs, Quantum tunneling, Quantum coherence, Nanoscale devices, Energy efficiency, Quantum state manipulation.

INTRODUCTION

The expansion of computer technology has reached a significant stage, as quantum mechanics collides with conventional semiconductor devices. The new applications of quantum computing offer an alternative to traditional systems that are reaching a dead end in terms of speed and efficiency. The most important

element of this change is field-effect transistors (FETs), which are fundamental components of typical electronic circuits. Their construction, functions, and the way they would integrate into quantum systems are matters of study, particularly in terms of their efficiency and the possibility of smaller sizes. Both graphene and complex oxide structures demonstrate that new materials can be optimized to increase qubit stability and control in the new FET designs. To give an overview of various semiconductor setups, an easy description of fundamental concepts upon which these devices rely, and the significance to future quantum computing technology is relevant. The relationship between quantum computing and FETs is a major breakthrough in computing power and efficiency.

Definition of Quantum Computing

The invention of computational means has reached a significant stage with the emergence of quantum computing, which applies quantum-mechanical concepts to process information differently. In comparison with regular computing, where the smallest unit of data is a bit (0s and 1s), quantum computing uses quantum bits, or qubits, which can be in a mixture of states simultaneously as a result of superposition and entanglement. The computing power is significantly enhanced with this ability, and complex problems can now be solved that cannot be solved by classical computing. Quantum mechanics is increasingly significant in new technology, particularly in the fabrication of Field-Effect Transistors (FETs) as the devices become smaller. The integration of quantum effects into solid-state devices is underway with improved materials and production methods, reinforcing the relationship between quantum computing and future semiconductor technologies [1, 2].

Overview of Field-Effect Transistors (FETs)

Over the last few years, field-effect transistors (FETs) evolved considerably and contributed to the massive enhancement of semiconductor technology, particularly in quantum computing applications. With high-leakage-power CMOS technology nearing its peak, alternatives, such as Tunnel FETs (TFETs) and Negative-Capacitance FETs (NCFETs), are emerging. They hope to increase energy efficiency by reducing the sub-threshold swing (SS) to a lower value than the standard threshold of 60m V/decimeter at room temperature [3, 4]. Single-dopant MOSFETs, such as silicon-on-insulator devices, have been investigated recently, highlighting significant progress in atomic-scale control, useful for quantum applications [3 - 5]. Such FETs can be scaled to quantum computing designs where higher performance and reduced sizes are of importance, thereby transforming the capabilities of electronics. The outcome of this development

CHAPTER 6

A Comprehensive Review of the Evolution of Isfet-based Biosensors for Glucose Detection in Urine, Analysing their Technological Advancements, Challenges, and Future Directions

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Abstract: Over the last 20 years, ISFET (Ion Sensitive Field Effect Transistor) biosensors have been recognized to be the most important technology in detecting glucose in non-invasive ways in urine, changing the way blood glucose concentration is measured. In this paper, an attempt has been made to present the development of ISFET-type glucose biosensors as attributed to advances in nanoscience, surface functionalization techniques, and sensor miniaturization, which improved the ability of the sensors to be sensitive, selective, and stable. More specifically, we focus on how graphene, metal oxides, and carbon nanotubes have been used to increase the surface area of ISFET sensors so that there is more contact with glucose molecules, thereby improving the sensitivity.

Another serious problem which is obtained with ISFET-based glucose sensors is related to the detection of glucose due to other constituents like urea and creatinine present in urine, which affects the accurate measurement of glucose. Examples of how these challenges have been overcome are discussed in this paper, including surface modification with glucose oxidase enzymes, and the use of molecularly imprinted polymers (MIPs) for enhanced specificity. The paper also discusses the issue of biofouling and the stability of the sensors caused by biological exposure for long periods, and how it can be solved with different coatings and more rigid materials.

The paper talks about making ISFET sensors smaller, which allows them to fit into wearable and implantable gadgets for tracking glucose levels all the time. We look at products on the market and examples from clinical studies to show how ISFET technology is being applied in real life. Lastly, we mention future research paths, such as using artificial intelligence (AI) and machine learning (ML) for better data processing and less intrusive glucose monitoring methods. This review stresses the

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importance of ongoing improvements in ISFET glucose detection to address current issues, reduce costs, and increase acceptance in clinical settings.

Keywords: ISFET biosensors, Glucose detection in urine, Nanomaterials (Graphene, CNTs, ZnO), Surface functionalization, Wearable glucose sensors.

INTRODUCTION

Background on Glucose Detection

Diabetes mellitus has acquired major public health implications affecting millions across the globe. Glucose monitoring proves to be an essential factor in controlling diabetes, for it enables patients, as well as healthcare providers, to decide on time-bound insulin therapy and the adjustments required in the patients' lifestyles. Glucose levels are generally measured by testing blood samples. This method is considered invasive, notably because it involves finger pricks, even though it is the most accurate means of finding glucose levels in the blood. However, for patients who have to undergo continuous monitoring, it is painful and unpleasant [1, 2].

Urine glucose monitoring is an alternative approach to glucose monitoring via a less invasive method that has become increasingly popular over the years. Previously, urine glucose detection was used only as complimentary blood glucose testing. Under normal circumstances, glucose should not be present in the urine, but for diabetic patients, hyperglycemia causes the excretion of glucose in urine whenever the blood glucose level surpasses the renal threshold. While urine glucose monitoring does not give real-time feedback compared to blood glucose measurements, it is perceived as more diagnostic, making the tool more useful in general surveillance and monitoring among diabetic patients.

In some cases, conventional urine glucose detection approaches, i.e., dipsticks or chemical assays, are sensitive to other urine components and sometimes show cross-reactivity. However, within the domain of biosensors, specifically ISFET-based sensors, it is possible to circumvent those challenges and achieve more reliable real-time glucose monitoring.

ISFET Biosensors

The Ion-Sensitive Field-Effect Transistor (ISFET) was first introduced in the early 1970s as a pH sensor, capable of detecting ion concentrations in various solutions. ISFET operates similarly to MOSFET (Metal-Oxide-Semiconductor FET) devices, but instead of using a metal gate, it utilizes a reference electrode immersed in the solution. Changes in the ion concentration modulate the

transistor's threshold voltage, providing a measurable signal [3]. Fig. (**1**) depicts the ISFET structure, in which the gate is replaced by an electrolyte and a reference electrode to enable ion sensing. From ISFET's inception, the technology has been modified and incorporated into several biochemical detection systems, such as glucose monitoring. ISFET sensors are ideal for real-time and portable monitoring systems due to their small size, low power consumption, and rapid response time. Glucose is detected using an ISFET-based sensor whereby the sensor was inserted into blood and acted on glucose oxidase, which helped break down glucose into hydrogen peroxide, which resulted in a local pH shift to the sites in a manner readable by the ISFET [4].

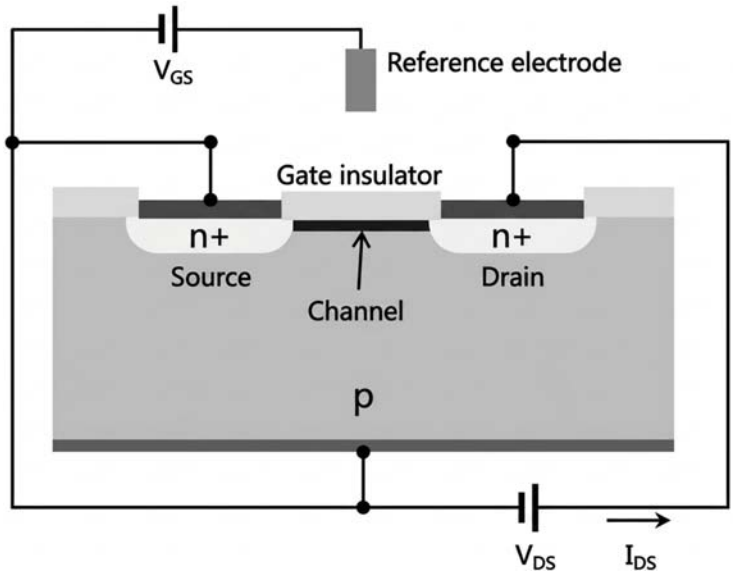

Fig. (1). Structure of ISFET [8].

ISFET sensors, being microfabricated, started to be modified for the detection of glucose in urine for a more complex environment. Glucose detection becomes more difficult in the urine due to other ions (*e.g.*, sodium, potassium, urea) that could inhibit the response of the sensor. However, there are still significant challenges that need to be overcome, great advances have been made in nanomaterials and surface functionalization strategies to improve the selectivity and sensitivity of the ISFET sensor for urine glucose detection [5 - 7].

Objectives

The objective of this chapter is to consolidate literature about the development of ISFET-based biosensors for glucose detection in urine, especially their advantages

CHAPTER 7

Design and Analysis of CMOS SRAM Cells for Read, Write, and SNM Optimization Using Even-Odd Transistor Configuration

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Abstract: This chapter examines 6T, 8T, and 10T SRAM cell designs and their compatibility with 45nm, 90nm, and 180nm technological nodes. It primarily examines the power consumption, speed, and signal strength of SRAM cell designs. The study uses tools to see how each SRAM cell design works under different conditions. For read, write, and hold operations of the SRAM cell designs, it compares the signal to the noise margin. The findings aid in understanding the advantages and disadvantages of each design, using technologies such as 45nm, 90nm, and 180nm to guide future advancements in memory technology.

Keywords: SRAM cell, Power, Delay, Read delay, Write delay, Hold margin, SNM.

INTRODUCTION

SRAM is a type of memory that does not require constant refreshing to retain data. This implies it can swiftly access the data it stores. SRAM is crucial for the design of power-hungry computer chips [1, 2]. Microprocessors, game consoles, portable electronics, and other compact devices frequently contain SRAM. SRAM, a type of memory known as cache, is typically used in these devices to help the chip retain information it frequently accesses. Memory is a great option for a variety of purposes, as it offers features such as data access, low power consumption, and the ability to avoid constant refreshes [3, 4]. Today, static RAM is part of computer chips and is used to store data that the chip needs to access quickly. Static RAM becomes more difficult to maintain as technology shrinks. Static RAM becomes less stable, more susceptible to interference, and uses power while not in use, among other issues. Researchers have developed static RAM

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designs that differ from the standard six-transistor design to address these issues. The 6T, 7T, 8T, 9T, and 10T static RAM bitcell topologies will all be compared in this chapter. The study examines factors like stability, reading and writing time, power consumption, overall power consumption, and space usage. This makes it easier for us to understand what we give up when we choose one type of cell over another. SRAM is ideal for systems that require quick responses because of its exceptional speed in retrieving the information we need. When the power is cut off, SRAM memory forgets what it has learned. Even when not in use, SRAM consumes some power. When in use, it often consumes less power than DRAM. SRAM is an option due to its speed and low power consumption. It is also used in embedded applications where speed and energy economy are crucial, as well as networking hardware such as switches and routers.

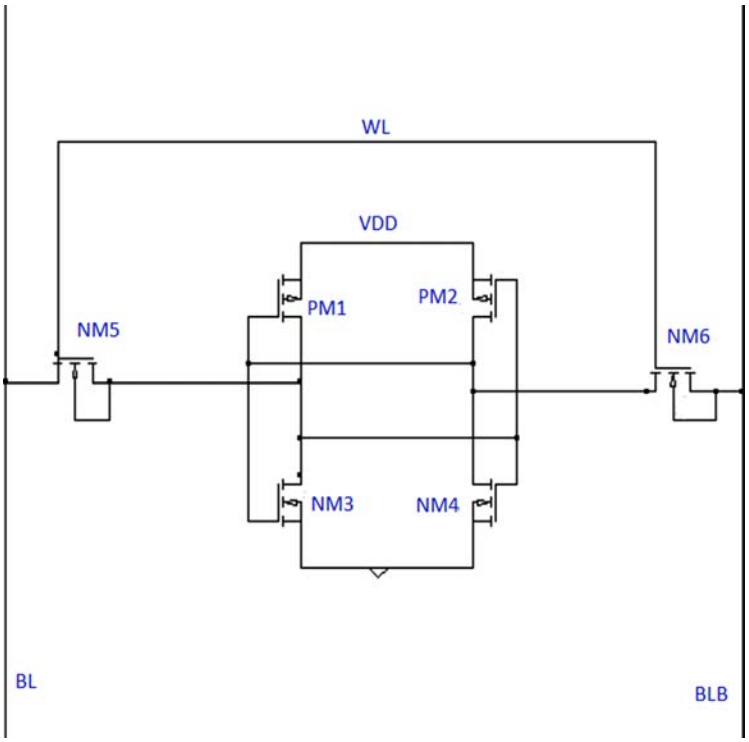

Fig. (1). Circuits diagram of a 6 T SRAM Cell.

The 6T SRAM cell is what people usually use to store a bit of data in random-access memory. This cell works because it maintains stability through internal feedback. In Fig. (**1**), you can see that the 6T SRAM cell has two CMOS inverters connected to retain information. The 6T SRAM cell can hold a logic 1 or a logic 0 for a long time, as long as it receives the power it needs. The 6T SRAM cell is

very good at doing this. These inverters help store information and keep it safe when there are no external signals. The storage nodes are called Q and QB. They show the true and complementary outputs of the inverters.

There are two transistors, M5 and M6, that connect these nodes to the bit lines BL and BLB. The word line (WL) determines whether a cell can be accessed. It is, like a switch that controls the operation of the transistors M5 and M6. It determines whether the cell is open or closed based on the word line [5, 6]. When the word line is driven high (WL = 1), the access transistors turn on, enabling the connection between the internal nodes and the bit lines. This state allows data to be written into or read from the cell. When WL is low (WL = 0), the cell is disconnected from the bit lines, placing it in a hold condition where the cross-coupled inverters independently retain the stored data without external influence. The reason is that the data can be stored without constant refreshing. When you want to write some data, the bit lines BL and BLB are given voltage levels that match the data you want to write. If you turn on WL, these voltage levels are strong enough to override the cell's feedback loop, causing the values stored in Q and QB to be updated. The bit lines are like the path that the new data takes to get into the cell when you are writing something. This means the old stored value can be replaced with some information. If BL is driven low and BLB is high, Q becomes '0' and QB becomes '1'; reversing these signals results in the opposite state. Proper write operation requires that the access transistors be strong enough to override the existing latch state. Before any read or write operation, the bit lines are typically precharged to a known voltage level, usually V_{DD}. Precharge ensures proper sensing operation, prevents signal disturbance, and avoids conflicts between internal and external signals. When we read something from memory, the memory gets ready first. Then the word line is turned on. The bit line connected to the place with a zero starts to lose power slightly due to the pull-down network. The other bit line connected to the place with a 1 in it stays close to the power supply. The sense amplifier detects the power difference and determines whether the stored value is 1 or 0 [7, 8]. Accurate sensing of this differential voltage is essential to avoid read failures. A disturbance or voltage rise at node Q or QB during the read operation may force an unintended flip in the latch, resulting in erroneous data output.

When we write something, we need to change the value stored. To do this, we intentionally make one of the bit lines touch the ground. This makes a voltage difference. If we make WL high, it pulls node Q or QB low, turning off the pull-up transistor, and the other node can change state. For example, if we make BL low, this will affect PM1 and NM1. It will drive the node below the point at which it can work. This will turn off PM2. Turn on NM2. So, we get the logic level. This controlled process ensures that the cell is updated reliably. Overall, the

CHAPTER 8

Advancements in Power Optimization for CMOS Complementary Transistor Configurations

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Abstract: This chapter focusses on a comparison of SRAM cell design with six, eight, and ten cell designs and discusses them in the context of various technology nodes, such as 45nm, 90nm, and 180nm. The emphasis is put on essential performance aspects, such as power consumption, speed, and signal quality. Through the application of complex analyzing tools, the study examines the performance of each design under the various conditions, specifically the signal-to-noise margin when performing the read, write, and hold operations. The findings are useful in indicating the strengths and weaknesses of each design, giving an insight into the possible impact of different technologies on the future of memory technology.

Keywords: SRAM Cell, Power, Delay, Read Delay, Write Delay, Hold Margin, SNM.

INTRODUCTION

SRAM is recognized as a type of memory that is special, and that has several advantages, including the possibility to access each bit individually and the absence of a periodic refresh need. It is particularly significant to low-power design within VLSI systems, and particularly because of its significant role in the detailed design of high-efficiency chips with low power consumption [1 - 5]. This complexity attracts the interest of the challenges in balancing efficiency and performance in energy. SRAM is a major constituent of cache and memory applications that is commonly implemented in gaming devices, microprocessors, and portable electronics [6]. It is a choice of many applications in various technologies that operate on some of the attributes, such as the rapid transfer of data, minimal power supply, and the lack of periodic refreshments [7 - 12]. On-chip data storage and cache memory in the current integrated circuits consist of

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static RAM. SRAM is, however, more challenged with more technology nodes being reduced, including reduced stability, higher leakage currents, and being predisposed to various noise factors. To solve these issues, researchers have investigated alternative designs of SRAM cells beyond the traditional 6-transistor (6T) design. This chapter gives a thorough comparison of SRAM cells built with 6T, 7T, 8T, 9T, and 10T architectures. In this paper, the author seeks to explain the trade-offs associated with each design by referring to critical performance indicators such as stability, read delay/power, write delay/power, power consumption, and area efficiency [13 - 16]. The speed of SRAM access makes it suitable for situations where quick data access is required. However, like other types of RAM, SRAM is volatile, so when power is disconnected, the data stored in it will be lost. SRAM consumes power when unused due to transistor leakage, though it generally consumes less power when active than DRAM. Also, SRAM can be used in networking devices such as switches and routers and embedded systems, where its speed and low power consumption come in especially handy [17 - 25].

STRUCTURE AND RESULT DISCUSSION

An essential part of static random-access memory (SRAM) for data storage is a 6T SRAM cell. The different nodes, control signals, and parts connected to the SRAM cell are shown in Fig. (**1**). Two coupled CMOS inverters that function as NOT gates make up the cell. Transistors NM5 and M6 control access to the memory section, which is connected to the bit lines BL and BLB. These access transistors permit communication with the bit lines when the word line (WL) is set to one (enabled); on the other hand, the memory stays in a hold state when WL is set to zero (disabled). The BL and BLB lines, which act as input lines in this situation, are manipulated to input data into the memory during a write operation. On the other hand, these lines serve as output lines during a read operation. Furthermore, SRAM cells frequently undergo precharging, which guarantees that the bit lines are in a known state before any read or write operations [26 - 31]. This precharging procedure preserves signal integrity and helps avoid contention problems. Both read and write operations make use of the WL line. Voltage increases that could cause unexpected output states in the other inverter can occasionally be used to identify performance issues during read operations at the Q/QB inverter nodes. The memory segment must maintain certain values in these circumstances, such as Q being high (1) and QB being low (0), or vice versa. When the word line (WL) is enabled to one (1), the access transistors are activated, enabling the bit lines BL and BLB to operate as output lines during a read operation. The bit lines are precharged using the voltage Vdd as a result of the voltage differential. The storage node (Q or QB) with a value of 0 discharges, which is subsequently picked up by a sense amplifier to finish the read process. In

a similar manner, values are assigned to Q and QB during a write operation. The bit lines BL and BLB, which function as input lines, can be accessed by turning on WL. In order to effectively manage these lines, one of the bit lines is grounded. This grounding produces a voltage difference that influences PM1. PM2 is off when the voltage is lower than the minimum threshold of M2, and generates the desired output. It is a sequence of events that enables the write action in the memory [32 - 38].

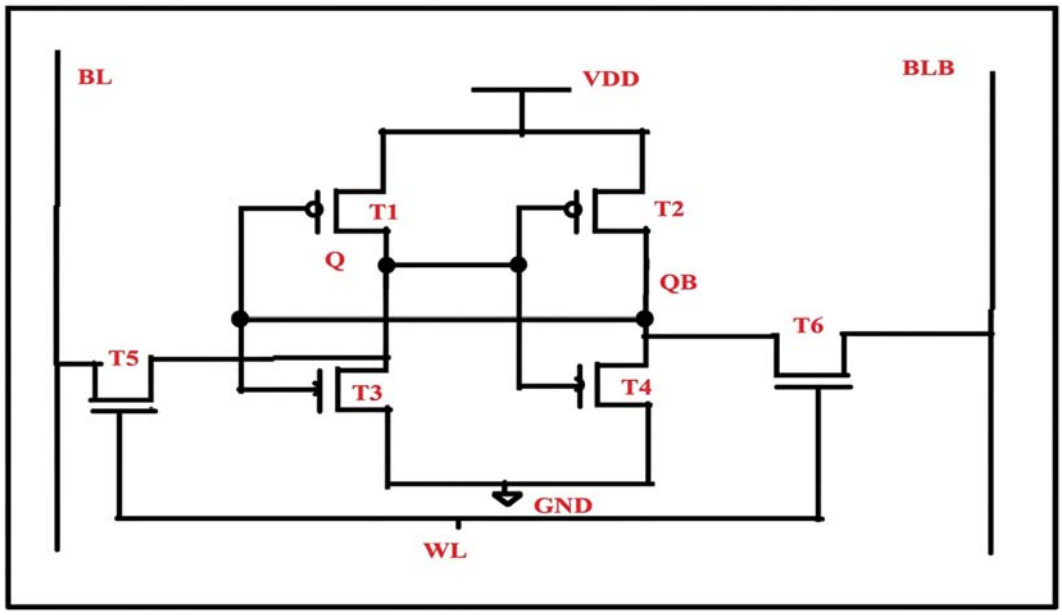

Fig. (1). Circuit diagram of a 6 T SRAM Cell.

A thorough comparative analysis is conducted using the 8T SRAM cell architecture, which is depicted in Fig. (**2**). According to this architecture, transistors M5 and M6 are linked to inverters that follow each other. The read buffer is applied to transistors M7 and M8. When read processes utilize read word lines (RWL), word lines (WWL) are utilized in write processes. The circuit footprint of the 8T SRAM cell is larger than the 6T SRAM cell because the former one incorporates two more transistors, which contribute significantly to the consumption of the System-on-Chip (SoC) space. To finalize the entire design, the two types of SRAM cells also have components such as a write driver, a sensing amplifier, and precharge circuitry. Parameters such as write delay and read delay are significant when it comes to evaluating the performance of SRAM.

CHAPTER 9

An Investigation of Junctionless Multigate Device and Its Application as 6T, 8T SRAM Cell at Sub-20 nm Technology Node

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Abstract: In the electronic industry, the development of efficient FET devices with smaller feature sizes, lower power consumption, and improved performance has intensified competition. The key challenge remains in miniaturizing and creating energy-efficient devices. Multi-gate technologies like FinFETs have become a promising solution for further scaling, offering a compact design and superior current control. As technology continuous to progress, its importance increases, especially in narrowing the performance gap between processors and main memory. Therefore, SRAM has an important role in determining system performance, reliability, and power consumption. This chapter focuses on the design of 6T and 8T SRAM cells using a FinFET device. The key considerations in SRAM cell design include size, noise margin, and access time. Therefore, this chapter also explores SiGe-based SRAM cells, analysing their performance regarding noise margin and delay.

Keywords: FinFET-based SRAM, Junctionless finFET (JL-FinFET), Short-channel effects (SCEs), Low-power memory design.

INTRODUCTION

As the channel dimensions of conventional MOS transistors shrink to the deep nanoscale, below 20 nm, the continued advancement of Moore's law leads to undesirable short-channel effects (SCEs). These effects include higher leakage current, higher "Subthreshold Swing (SS)", greater "Drain Induced Barrier Lowering (DIBL)", and rising manufacturing cost [1 - 3]. The SS measures how quickly a device turns off below the threshold voltage (V_{th}) (V_{th} is the minimum gate voltage required to start conduction) [4, 5]. Ideally, SS should be around 60

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mV/dec at room temperature, but this varies with the temperature. An "ideal" SS allows the >device to >switch OFF >rapidly, reducing >the leakage >current >and preserving the drive current. However, as transistor dimensions scale down, the device's performance deteriorates; SS flattens, V_{th} decreases, and the device becomes harder to turn OFF by reducing gate-source voltage (V_{GS}). DIBL is a phenomenon where drain potential further depletes the channel, worsens at nanoscale levels, resulting in inversion at lower V_{th}, increased leakage, and high static power dissipation. To continue scaling devices beyond physical limits, new device structures and materials are being explored. These advancements fall into two categories: (1) enhancing the CMOS platform by integrating additional technologies ("More Moore") and (2) introducing innovative computing paradigms or new device architectures ("Beyond CMOS") [6]. Beyond CMOS technologies may offer necessary breakthroughs in device architecture and techniques for the next era of computing [6]. Fig. (**1**) shows an overview of the scaling trends for beyond CMOS and More-Moore.

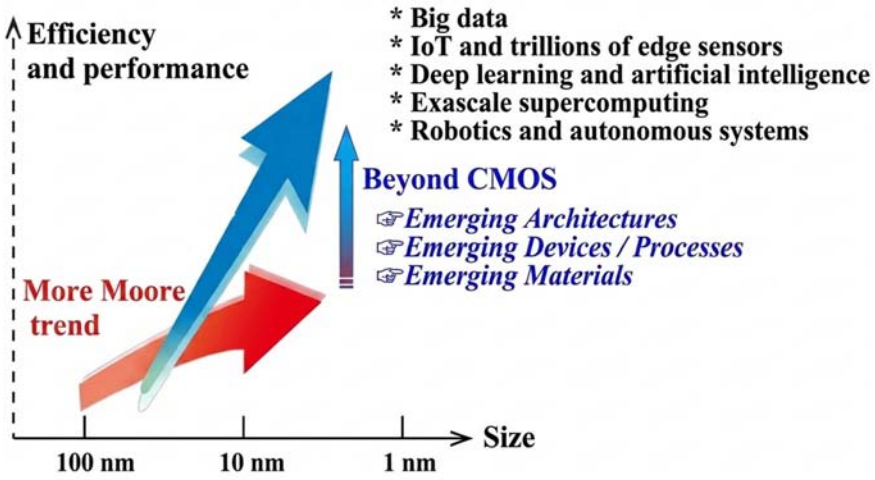

Fig. (1). Scaling trend and beyond CMOS scope [6].

This chapter provides an overview of the junctionless FinFET devices and compares them with the inversion mode device. This chapter also explores the application of FinFET devices as an application in designing SRAM cells. Furthermore, the analysis of 6T and 8T SRAM cells based on a FinFET device consisting of a stack channel (Si-SiGe-Si) is performed.

MULTI-GATE DEVICES

In highly scaled MOSFETs, the drain voltage can affect the channel's electrostatics, causing the gate to lose control over it. This limits the gate's ability to fully switch OFF the device in OFF mode, leading to an increase in OFF current (I_{OFF}) between the source and drain [7, 8]. One way to address this issue is by using thinner gate oxides and high-dielectric (high-k) materials, which increase the gate-source capacitance (C_{GS}). However, this approach has limitations due to the rise in the gate-induced drain leakage (GIDL) [7, 8]. Multi-gate FETs serve as an alternative to traditional FETs, providing larger CGS and better isolation of the drain potential from the channel. These devices outperform planar FETs in controlling short-channel effects (SCEs) like SS and DIBL, resulting in less degradation in V_{th} and lower I_{OFF} with device scaling. Among multi-gate structures, double-gate and tri-gate devices are preferred over conventional MOSFETs for their superior ability to reduce SCEs [8 - 10]. Further research has been conducted on multi-gate devices, including Tunnel FETs (TFETs), and FinFETs [11 - 14].

FinFETs have attracted significant attention in recent decades due to their superior resistance to SCEs compared to conventional (planar) MOSFETs [15]. Fig. (**2**) depicts the differentiation between a planar MOSFET with a horizontal channel and a FinFET with verticle channel. In the planar device, the key parameters are gate length (L_G) and device width (W), whereas in FinFETs, the critical parameters are L_G, fin height (H_{fin}), and fin thickness (t_{fin}) [16]. The FinFET structure gives rise to a unique characteristic known as "width quantization", which means the FinFET width depends on fin height and thickness. The effective fin width (W_{eff}) is calculated as: $W_{eff}=2H_{fin}+t_{fin}$ [17, 18].

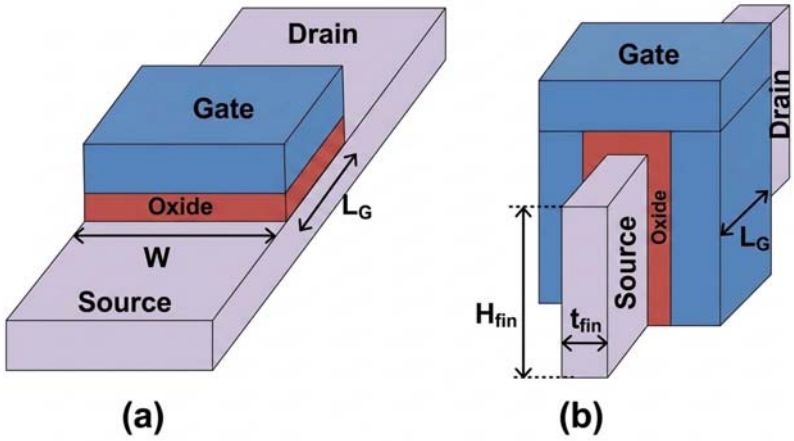

Fig. (2). (a) Planar MOSFET (b) FinFET device.

CHAPTER 10

A Comparative Study of Split-Gate *vs.* Non-Split Gate Doping-Less Heterojunction Tunnel FET: Performance and Design Insights

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Abstract: In this chapter, an analysis of a split-gate, doping-free heterojunction tunnel field-effect transistor (SG-DG-HJ-TFET) compared with a heterojunction tunnel field-effect transistor with a non-split-gate (NSG) architecture will be presented. The Doping-Free Tunnel Field-Effect Transistor (DF-TFET) is a promising next-generation design, offering robustness against random dopant fluctuations and eliminating the need for high-temperature processing and expensive annealing. The performance of both configurations is analyzed and compared in terms of DC performance. Parameters such as drain current, electric field distribution, surface potential, sub-threshold swing (SS), current, *etc.*, are evaluated during this evaluation. The temperature dependency of both the TFET architectures is compared and reported in this work. The Silvaco ATLAS technology is used for two-dimensional design simulation to implement the suggested design. The fabrication flow of the proposed SG-DG-HJ-TFET is also described in detail.

Keywords: Band-to-band tunneling (BTBT), DopingLess, Potential, Short channel effects (SCEs), TFET.

INTRODUCTION

Reducing device power consumption requires a significant drop in the supply voltage (V_{DD}). To retain the same ON current (I_{ON}), the decrease in the threshold voltage (V_{TH}) is also necessary so that there is sufficient overdrive voltage ($V_{DD} - V_{TH}$) maintained. But when we reduce V_{DD} and V_{TH}, the OFF current (I_{OFF}) increases noticeably.

This surge in I_{OFF} is inevitable due to the persistent Sub-threshold Swing (SS) of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) with a theore-

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tical minimal threshold of 60 millivolts/decade at ambient temperatures. Because of such thermionic limitations on the MOSFETs' Sub-threshold Swing (SS), contemporary electronic devices that rely on MOSFET technology have trouble operating at reduced power supplies [1, 2]. A solution to overcome this problem is by suggesting devices with SS scaling <60 mV/decade. Tunnel Field-Effect Transistors (TFETs) are emerging as a promising alternative to conventional CMOS logic devices due to their unique characteristics [3 - 5]. Unlike MOSFETs, TFETs use BTBT as the primary carrier-injection mechanism rather than thermionic emission. This distinction allows TFETs to offer a variable and scalable sub-threshold Swing (SS) that is lower than 60 mV/decade [6 - 8]. Nevertheless, limitations of TFETs, including low I_{ON} (drain current) and ambipolarity, continue to hinder their potential to replace conventional MOSFETs. TFETs exhibit lower I_{ON} values than MOSFETs, which poses a significant obstacle to their overall performance and suitability as a replacement technology.

The ON-state performance of TFETs has been improved by a number of methods that emphasize both structural and material-based techniques [9 - 14]. These solutions aim to enhance the overall efficacy and functionality of TFET devices. An alternative approach, known as the charge-plasma-based structure, has been documented to enhance the effectiveness of TFET devices [15 - 17]. This structure avoids conventional doping of the source and drain regions. As an alternative, the charge concentration is brought about by introducing metal into contact with the semiconductor contacts. However, specific conditions related to the work function and film thickness must be met for this method to be effective. We present a new design in this work, termed the split-gate doping-less heterojunction TFET (SG-DL-HJ HTFET). A split-gate configuration significantly improves the ON-state performance of the dual-gate Tunnel Field-Effect Transistor.

The operational principle of TFET is explained in Section II. In Section III, the device's design and simulator details are presented. The findings and discussion are presented in Section IV. Section V reports on and discusses the results of the sensitivity analysis. Section V concludes this chapter.

New Approaches for Upcoming Technology Generations

Changes in channel material and topologies are essential for tackling the growing trajectory of static energy use for semiconducting devices at the forthcoming technological node. The following innovations are considered the most viable options to continue scaling technology down to dimensions in the nanometer range:

1. The next step in the scalability plan of action, based on 2015 ITRS estimates, is to replace the stretched silicon channels in MOSFETs with materials that have excellent mobility. This transition poses several challenges that need to be addressed. These challenges include enhancing the interface across large-K materials and Ge-III-V materials, reducing band-to-band tunnelling within narrow bandgap materials, and achieving exceptionally large-scale integration utilising a silicon medium's scalable process flow. These are just a few illustrations of the obstacles that must be overcome in this endeavor [18, 19].

1. Nanowires (NWs) offer a promising avenue for replacing traditional planar MOSFET channels, potentially enabling a further reduction in technology node size. This is achievable because NWs can be manufactured with diameters in the nanometer range [20]. NWs are particularly well-suited for gate- all-around structures, which have the potential to mitigate short-channel effects. Their vertical growth orientation aligns with the future trend of vertically integrating devices on semiconductor chips. To ensure the growth of defect-free nanowires, improvements in circuit yields and consistency are required. Additionally, supposing the transfer of NWs to other platforms becomes necessary, precise positioning becomes crucial. To avoid surface irregularities and defects, it is essential to develop effective surface treatment and passivation techniques.
2. Carbon Nanotubes (CNTs) are considered a promising choice for technology nodes below 10 nanometers due to their extremely thin bodies, approximately 1 nanometer in diameter. Compared to silicon, CNT-FETs can provide enhanced electron and hole mobility in the channel, especially at room temperature. However, challenges exist in terms of achieving VLSI integration with CNTs, including the need to purify and sort CNTs to ensure a relatively uniform diameter distribution [21].
3. Graphene Field-Effect Transistors (GFETs) hold significant potential for RF design due to their superior carrier mobility compared to CNTs. They enable the expansion of faster transistors with smaller dimensions. Graphene, which represents a solitary atomic layer, is essentially a zero-bandgap semiconductor. Consequently, the primary focus of research in this area is on developing effective methods to introduce a bandgap. This is crucial for achieving a substantial current gain (I_{ON}/I_{OFF}) suitable for radio-frequency and analogue applications [22].
4. Tunnel Field-Effect Transistors (TFETs) are highly regarded as among the most advanced technological advancements for applications requiring unelevated power and modest effectiveness as a result of their distinct electrically properties [23].

CHAPTER 11

Optimizing DC Parameters in Hetero-Stacked Source Tunneling Field-Effect Transistor

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Abstract: This chapter studies a hetero-stacked source n-type TFET (HSS-nTFET) using TCAD simulations. The device uses a stacked-source structure with gate–source overlap to improve tunneling. This design increases the electric field at the source–channel junction and reduces the tunneling width, which supports higher current conduction. The electrical performance is analyzed by varying the source stack materials and key device dimensions. Based on the simulation results, the proposed HSS-nTFET achieves an average subthreshold swing of about 20 mV/dec, and an I_{ON}/I_{OFF} ratio on the order of 10^{12}. The effect of different gate dielectric materials is also examined, showing that high-k dielectrics improve the ON current and switching performance.

Keywords: Heterostack, Drain underlap, Band to band tunneling (BTBT), Stack source engineering, Subthreshold swing.

INTRODUCTION

Over the past few years, there has been a continuous trend toward downsizing CMOS chips, pushing physical boundaries into the realm of nanoelectronic technology [1]. This scaling focuses on improving device performance, reducing power consumption, and increasing IC density. Even with nanoscale scaling, CMOS faces challenges such as short-channel effects, high leakage current, power loss, and threshold voltage drop. Conventional MOSFETs have a subthreshold swing above 60 mV/decade because of thermionic emission [2, 3]. This limitation has led to interest in TFETs as alternative devices. TFETs use band-to-band tunneling (BTBT) to overcome the 60 mV/decade limit at room temperature. They also provide low off-current, making them suitable for ultra-low-power applications [4 - 6]. Conventional TFETs face challenges such as low ON current and unwanted OFF-state current due to ambipolarity [7 - 9]. Improving these

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aspects is important for higher drive current and better circuit performance. For comparison, MOSFETs have a minimum subthreshold swing of 60 mV/decade at room temperature and a very low I_{ON}/I_{OFF} ratio [10]. In contrast, TFETs use tunneling to achieve SS values below 60 mV/decade. To improve their performance, several device designs and strategies have been proposed [11 - 15]. Adding low-bandgap materials to heterojunction TFETs can increase ON current and reduce leakage current. Group III-nitrides such as InN, which has a bandgap of 0.7 eV, are commonly used in these devices [16]. By reducing the tunneling width and causing band bending, InN helps increase the ON current. This work studies a lateral n-channel hetero-stacked TFET (HSS-nTFET) using InN to improve device performance. The HSS-nTFET is expected to show a better SS and lower leakage current.

The chapter is divided into five sections. The first section introduces the study. Section 2 shows the cross-sectional view of the proposed TFET and the main parameters. Section 3 presents the simulation results and analysis. Section 4 compares the results with previous works. The final section provides conclusions.

DEVICE STRUCTURE AND PARAMETER SELECTION

Fig. (**1a**) shows the cross-sectional view of the proposed HSS-nTFET. The device has a two-dimensional lateral n-channel structure. It is similar to a conventional TFET, but a stacked source is used instead of a single source region. In the source region of the n-channel HSS-TFET, two different materials are stacked. Si forms the first layer, while InN is used as the second layer. The source region is formed using three layers. The top and bottom layers are Si with a bandgap of 1.1 eV, while the middle layer is InN with a lower bandgap of 0.7 eV. Silicon is also used for the channel and drain regions to limit leakage current. This layered source structure improves band-to-band tunneling and increases the ON current. A higher electric field is observed at the source–channel junction due to the stacked source. Ambipolar current may appear in n-type TFETs under negative gate bias due to hole tunneling from the drain side. So, a gate–drain underlap is applied to reduce this effect. An optimized gate–source overlap is used to increase the effective tunneling region. This overlap increases the local charge density and facilitates a faster change in channel potential [17]. InN is a III–V direct band-gap semiconductor with a bandgap of about 0.7 eV. When used in the source stack, it reduces band bending and narrows the tunneling width, thereby increasing the ON current. Compared with other III–V materials, InN shows strong electron accumulation at the surface. Device simulations were performed using the Synopsys TCAD Sentaurus tool [18]. The parameters used for the proposed device are listed in Table **1**. The P^+ InN source is doped at $1\times10^{21}cm^{-3}$, while the channel and drain doping are set to $1\times10^{17}cm^{-3}$ and 5×10^{18} cm^{-3}, respectively. An

undercut length of L_{UC} = 5 nm is applied in the i-Si channel, allowing the gate to overlap the source and underlap the drain. This design supports a steeper average subthreshold slope (SS_{avg}) and a higher I_{ON}. Fermi–Dirac statistics [18] are used to model the carrier distribution in the device. Furthermore, the Shockley-Read-Hall recombination model and the dynamic non-local band- to-band tunneling (BTBT) model are utilized. Throughout the entire tunneling path, a nonlocal BTBT model is applied. As the gate voltage increases, the channel conduction band moves downward. Band-to-band tunneling starts when the channel conduction band falls below the source valence band. For the proposed n-type HSS-TFET, a positive gate voltage places the device in the ON state. This causes band bending near the source–channel junction and allows efficient tunneling. The OFF-state current is evaluated at a gate voltage of 0 V, as shown in the energy band diagrams in Fig. (**1b** and **1c**) . In the ON state, the tunnel barrier width (λ_1) is smaller than in the OFF state (λ_0). This causes band-to-band tunneling to occur mainly along the path from A to A'. The red arrow shows the electron tunneling direction. Fig. (**2a**) and **2b**) display the volumetric electron generation rate in the device under the two bias conditions: i) OFF and ii) ON-state. Fig. (**3**) shows the transfer characteristics, which are compared with experimental data to validate the simulation models [19]. Fig. (**4**). illustrates the main steps in fabricating the proposed HSS-nTFET. A thick Si wafer is used for the channel. The source region is created by etching an L-shaped cut, followed by masking. The drain doping region is then formed through ion implantation. Within the L-shaped cut, the source stack region is developed by sequentially depositing Si in the first layer, InN in the second layer, and again Si in the third layer, with masking and subsequent ion implantation to form a P-doped source region. Subsequently, a thin oxide deposition layer is applied using the Atomic Layer Deposition (ALD) method [20]. This oxide layer is then shaped using selective etching. Finally, metal gate deposition is performed using sputtering technology and defining contacts at appropriate positions.

Table1. Physical parameters and doping of different regions.

Parameters	Values
Gate length(L_g)	25nm
Oxide thickness(T_{OX})	2nm
Channel length undercut(L_{UC})	5nm
P^+ stack source doping(N_A)	$1\times10^{21}cm^{-3}$
N channel doping	$1\times10^{17}cm^{-3}$
N+ drain doping(N_D)	$5\times10^{18}cm^{-3}$

The entry "Thickness of InN (T_InN) 4 nm" is currently appearing outside the table boundary. Kindly place this line properly within the table column along with the other parameters.

CHAPTER 12

Reliability and Sensitivity Analysis of TFET

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Abstract: This chapter concentrated on a comprehensive study of TFET with its optical application at three specific wavelengths. Initially, ionic radiation analysis was performed over the Ge-source double gate TFET to evaluate the parameter collected charge (Q_c) and bipolar gain (β). It generated a maximum bipolar gain of 71.6 at LET = 20 MeV.cm^2/mg. After this interface trap analysis, ZHP and hetero stack (HS) TFETs were analyzed, including their effects on the energy band and transfer characteristics. ZHP-TFET reported a major fluctuation in the drain current compared to HSTFET. Further, the impact of noise was evaluated at different frequencies on incorporating various trap effects. Finally, optical assessment of the TFET photo sensor was performed at wavelengths of 300, 500, and 700 nm. Here, HS TFET reported maximum spectral sensitivity (S_n) compared to ZHP-TFET at low gate voltages. The maximum spectral sensitivity of HS-TFET was observed as 421, and ZHP-TFET showed 125 maximum spectral sensitivity at a wavelength of 300 nm. The complete study of TFET was conducted at low supply voltage with minimal power dissipation.

Keywords: Ionic Radiation, Interface trap charge, Noise Analysis, Photo sensor.

INTRODUCTION

Semiconductor businesses are no longer limited to designing mobile devices, chips, and CPUs; they are also venturing into space applications. It is essential to conduct reliability analysis of field-effect transistors to assess their performance under adverse conditions. To address reliability factors, such as radiation [1 - 3], interface trap charges (ITCs) [4, 5], and noise analysis of TFETs [6 - 9] have been performed. Under the radiation effect, high-energy particles enter a semiconductor device, accumulating an extra electron-hole charge carrier. These extra carriers

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cause the device's regular functionality to be perturbed and result in radiation damage. However, the accumulation of trap charges [10] primarily between the semiconductor channel and gate oxide interface inhibits TFET operation. These ITCs arise from a mismatch between two surfaces during fabrication. Since the gate oxide layer follows the amorphous pattern of the layer while the silicon channel is made of crystalline form, the combination of these two layer result an unwanted trap impurities. The final analysis of TFET is application-oriented and includes the optical behavior of the device at a particular wavelength of incident light. Plenty of investigators have already examined the relationship between optical energy and FET-based photo sensors [11 - 14] in their respective fields. They are ideal for photo detectors due to the efficient power consumption, high quantum efficiency, and excellent sensitivity. Consequently, researchers are increasingly focused on FET-based optical detectors for optimal light detection at constant intensity. The literature contains reports on MOSFET-based optical sensors such as the PN Junction [15], Avalanche Photo sensor [16], and PIN Photo sensor [17]. Investigation demonstrates that PN junction and MOSFET devices [18] exhibit minimal photon absorption at excess power dissipation. In this regard, TFET has emerged as an alternative to other FET devices for light detection, offering a low operating voltage and a fast detection rate.

The initial study evaluated the impact of heavy ion radiation on the Ge-sourc--based double gate TFET. Analysis was carried out by calculating the collected charge (Q_C) as well as bipolar gain (β) for different linear energy transfer (LET) [19, 20] values. The impact of various types of trap impurities on the electrical characteristics of horizontal N^+ pocket ZHP-TFET and HS-TFET is further investigated. Subsequently, the optical characteristics of the hetero stack and Z-shape horizontal pocket TFETs were extracted at three different wavelengths in a specific range of the spectrum. The major optical figure of merit (FOMs), such as optical generation rate and spectral sensitivity (Sn) [21, 22], were determined for the corresponding optical device.

This chapter is divided into four sections. Section II provides the device architecture and simulation framework, preceded by the appropriate flow of the fabrication process for these TFETs. Section III describes the trap and optical properties of these TFET devices. Finally, Section IV concludes the chapter.

DEVICE DESIGN AND SIMULATION SETUP

To investigate the effect of heavy ion radiation, a Ge-source based double gate TFET [23, 24] has been considered with its dimensional parameter as illustrated in Fig. (**1a**). The availability of Ge in source side confirms diminished operating voltage of TFET, hence the device executes the fast switching operation and

minimum magnitude of leakage current. Further, TFET exhibits tunneling-based carrier conduction, which makes it more resistant to single-event effects (SEE). Fig. (**1b**) depicts the heavy-ion radiation image of the TFET with the corresponding radiation parameters. These essential parameters are: (i) the energy and type of ion, (ii) Angle of penetration, (iii) Penetration Length (L_{Max}), (iv) Radiation width (w), and (v) linear energy transfer (LET).

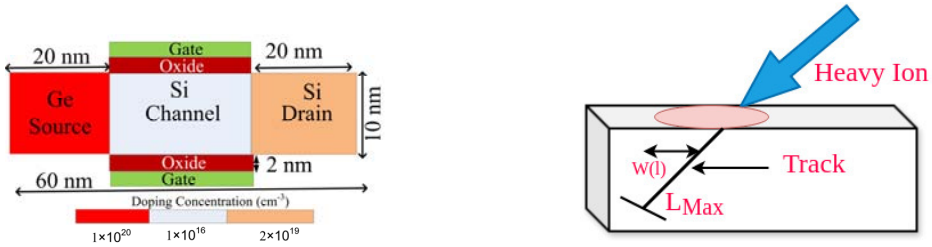

Fig. (1). (a) 2D Schematic of Ge Source Double Gate TFET and (b) Ge source DG-TFET under Heavy ion Radiation effect.

The device architecture of the N^+ pocket-based Z-shaped and stack TFET [24 - 26] as depicted in Fig. (**2a** & **2b**). The source side is heavily doped with P-type dopant; the drain region is doped with N-type dopant at 5×1018 cm-3 and the channel region is intrinsically doped at 1×10^{15} cm^{-3}. The ZHP-TFET exhibits one oxide layer on the source side and another silicon oxide region on the bottom side of the gate, confirming both lateral and vertical tunneling along the conductive regime.

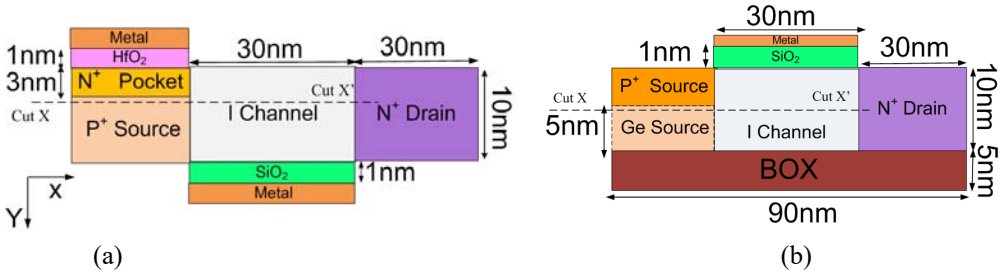

Fig. (2). Schematic of (a) ZHP and (b) HS TFET.

The Hetero stack TFET consists of a Ge source at the source side to operate the device at low V_{GS}. It consists of a silicon layer on the upper side and germanium on the bottom side for improved electrical characteristics. The impact of trap impurities is evaluated on various electrical parameters of TFETs for different trap charge concentrations. To analyze the impact of various ITCs, the acceptor type of traps impurities has been accounted for both uniform and Gaussian types

CHAPTER 13

Dielectric-Modulated Zinc-Oxide Nanostructured Thin Film Field Effect Transistor

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Abstract: This chapter discusses the design, simulation, and performance evaluation of a dielectric-modulated zinc oxide thin-film transistor (DM-ZnO-TFT) biosensor aimed at label-free biomolecule detection. The sensor exploits the dielectric modulation caused by biomolecules with different dielectric constants located within a nanocavity near the TFT's drain region. To improve stability and enhance molecular binding, a biocompatible Al_2O_3 layer along with a dielectric SiO_2 stack is incorporated. Through 2D TCAD simulations, key electrical parameters such as threshold voltage shift, drain current, surface potential, and transconductance were analyzed. The findings reveal a significant change in device behavior in response to biomolecules with dielectric constants ranging from 1 to 15, demonstrating the sensor's high sensitivity and real-time detection capabilities. This DM-ZnO-TFT biosensor offers a cost-effective, CMOS-compatible, and promising approach for future biomedical and environmental sensing technologies.

Keywords: Dielectric-modulated biosensor, Zinc oxide (ZnO), Thin-film transistor (TFT), TCAD simulation label-free detection, Biomolecule sensing.

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INTRODUCTION

BioFETs, or Field-effect transistor (FET)-based biosensors, have been a significant innovation in the biosensor field since their realization in 1980 [1]. They have broad applications in the agriculture, environment, food, and medical industries due to their signal amplification and unique biological recognition abilities. BioFETs consist of two primary components: the biological recognition element and the signal transduction. The biorecognition element uniquely recognizes and binds specific analytes. Signal transduction translates the biochemical interactions between the analyte and bioreceptor into readable signals. These components enable the creation of highly selective, sensitive, and reliable biosensors by integrating various bioactive materials. They offer fast response times, small size, low cost, lightweight, high reliability, and the ability to incorporate on-chip biosensor arrays for portable microanalysis systems [2, 3]. In BioFETs, the conventional gate metal is replaced with a biologically specific material. This modification enables the detection of target molecules present in the biofilm layer. The biofilm layer achieves this by modulating the channel conductivity of the FET. Ion-sensitive field-effect transistors (ISFETs), introduced in the 1970s, are a pioneering type of BioFET because of their small size, high input impedance, rapid response, and high sensitivity [4].

FET-based biosensors have seen widespread exploration, such as the catalyzed FET biosensors, which use biocatalysts like enzymes for binding and recognizing biological molecules [5, 6]. Enzyme-based ISFETs (ENFETs) are commonly used, where enzymes are stabilized on a gate insulator for specific substrate binding. The extended-gate FET (EGFET) introduced improvements over traditional ISFETs, offering advantages such as flexible gate area and ease of packaging [7, 8]. MOSFET (metal-oxide-semiconductor FET) biosensors are highly sensitive and operate on the principle of electrical biomolecule detection, modifying the electric field and affecting the drain current [9]. They have been used for detecting DNA-protein interactions and diagnosing diseases like Alzheimer's [10, 11]. Label-free detection techniques are common in various FET-based biosensors, offering advantages in simplicity and cost-effectiveness by integrating with CMOS technology.

TFT-based Biosensors

Thin-film transistor (TFT)-based biosensors are a significant class of biosensors that enable label-free detection of biomolecules. TFT biosensors consist of a thin film of semiconductor material deposited on an insulating substrate. TFTs do not require additional labeling of biomolecules, reducing the complexity and cost of the detection process [12]. TFT biosensors have been used to detect biomarkers

for diseases like birth asphyxia, sickle cell disease (SCD), traumatic brain injury, and stroke. Their high sensitivity and rapid detection capabilities make them suitable for monitoring critical health conditions. The large-area coverage and fast response times of TFT biosensors enable real-time monitoring of low-concentration protein analytes [13]. This capability is crucial in medical diagnostics, where timely information is critical for patient care. Additionally, solution-processed TFTs enable low-cost fabrication. These TFT-based biosensors are versatile and can be fabricated on a variety of substrates, including flexible materials, which broadens their potential applications in wearable and portable medical devices.

TFTs utilize various materials as the active semiconductor layer. Traditional materials include amorphous silicon and polycrystalline silicon, but these have limitations in terms of mobility and uniformity. Consequently, researchers have explored alternative materials such as carbon nanotubes, organic semiconductors, cadmium selenide, and metal halide perovskites. Among these, metal oxide-based semiconductors have gained significant attention due to their high carrier mobility, transparency, and stability. Zinc oxide (ZnO) is a widely used oxide semiconductor for TFTs [14]. ZnO offers outstanding electrical properties, such as high optical transparency, a large exciton binding energy of 60 meV, and a wide bandgap of 3.37 eV. Its ability to be deposited at low temperatures further enhances its suitability as an active layer material for thin-film transistor (TFT)-based biosensors. Moreover, ZnOs biocompatibility broadens its potential applications. ZnO-based TFT biosensors hold significant promise in diverse fields, including environmental monitoring, clinical diagnostics, and on-site detection [15]. Their high sensitivity, real-time monitoring capabilities, and cost-effectiveness make them ideal for various applications, providing efficient and reliable sensing solutions.

Dielectric Modulated Biosensors

Among FET-based biosensors, dielectric-modulated (DM) FETs have demonstrated superior sensitivity and are widely preferred for biosensing applications. The inclusion of nanocavities in DM-FETs provides ample space for effective biomolecule conjugation, thereby enhancing overall sensitivity. Choi *et al.* introduced the first DM-FET biosensor with nano-cavities for label-free biomolecule detection [16]. Since then, numerous dielectric-modulated FET biosensors with improved sensitivity have been developed [17]. Dielectric modulation is a technique that involves altering the dielectric properties within a device to control its electrical behavior. By incorporating biomolecules with varying dielectric constants into the cavity regions, a gradient is created, which influences the electric field distribution and the overall device response. When a

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Dielectric-Modulated Negative Capacitance Tunnel FET for Highly Sensitive Biosensing Applications

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Abstract: The biosensing potential of a ferroelectric negative capacitance biosensor tunnel field-effect transistor (FENCB-TFET) is investigated in this chapter using a dielectric modulation technique. The design features nanoscale pores near the source and drain regions to enhance the surface area available for biomolecule immobilisation, therefore directly enhancing electrostatic coupling. Adjustments in turn-on voltage, drain current sensitivity, and current switching ratio affect performance. We evaluated biomolecules with neutral, positive, and negative charges at the control layer and at the insulator edge under a range of dielectric conditions. The study takes into account practical limitations, such as partially filled holes caused by steric hindrance, in addition to perfect sensing. The findings show that the FENCB-TFET is a strong, extremely sensitive competitor for low-power, label-free biosensing.

Keywords: Biosensor, Dielectric modulation Sensitivity, Nano-cavity.

INTRODUCTION

Modern diagnostics, environmental monitoring, and biochemical sensing all require the ability to identify biomolecules at the nanoscale. Traditional methodologies often fail to deliver high reliability in these dimensions. Nanoscale electronic devices provide an alternative because of their tiny size, superior electrostatic control, and ability to directly convert biological interactions into electrical impulses [1]. Modern diagnostics, environmental monitoring, and biochemical sensing all demand the capacity to identify biomolecules on a nanoscale. Traditional methodologies usually fail to provide high reliability at these dimensions. Nanoscale electronic devices provide an alternative because of their tiny size, superior electrostatic control, and ability to transform biological

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interactions directly into electrical impulses [1]. However, traditional ion-sensitive FETs (ISFETs) have a blind spot: they have trouble detecting neutral molecules. This gap led to the development of dielectric-modulated FETs (DM-FETs). By employing nanocavities to detect variations in the dielectric constant within the cavity, these devices are able to recognise both charged and neutral objects [2 - 5]. Since then, tunnel FETs (TFETs) have become a powerful alternative to traditional CMOS. Their key feature is that they are suitable for low-power sensing as they can achieve a subthreshold swing below the thermal limit of mV/dec [6, 7].

Combining nanogaps with high-k dielectrics in TFETs sharpens sensitivity by increasing band-to-band tunnelling at the source. Tunnelling efficiency improves when biomolecules inhabit high-k cavities, allowing detection at extremely low concentrations [6 - 8]. According to a study, geometry is what determines performance. Targets near the source lower the tunnelling barrier, directly increasing sensitivity, as established by Narang *et al.* [8]. While others employed structural alterations, such as Gate-All-Around (GAA) designs, to improve electrostatic control [10, 11], Kanungo *et al.* further optimised these architectures [9]. A dual-metal gate method was successfully employed by Maradan *et al.* to control drain-induced effects [12]. Charge plasma approaches, which minimise random dopant oscillations without compromising performance, have been used to junctionless TFETs in order to streamline production [13]. Dwivedi *et al.* emphasised the transconductance-to-current ratio as an important factor [14], while Verma demonstrated that dual-metal designs enhance on-currents [15]. Noor *et al.* demonstrated this vertical TFET, proving that vertical TFETs outperform lateral ones because they have a larger tunnelling area [16]. Despite this, altering the dielectric constant remains a fundamental way for label-free detection [17, 18], which is frequently stabilised against temperature changes using charge plasma methods. Core-shell junctionless nanotube TFETs are another low-cost and scalable solution [19]. Recently, the emphasis has shifted to maximising efficiency metrics such as the current sensing ratio (CSR) and subthreshold swing (SS). Published SS values currently range from as low as mV/dec [20 - 24] to about mV/dec [25], validating TFETs' ultra-low-power capability [26].

The most recent innovation includes the use of ferroelectric materials. Ferroelectric negative capacitance provides better gate control and lower voltage operation, ushering in a new era of biosensor performance [26]. Building on previous advances, this chapter studies a ferroelectric negative capacitance dielectric-modulated TFET with nanocavities at the source and drain. To demonstrate its suitability for practical, label-free biosensing, we rigorously analyse this design under a variety of situations, including changing dielectrics,

biomolecular charges, and non-uniform distributions.

2D CONFIGURATION AND DEVICE DESCRIPTION

Fig. (**1**) depicts the FENCB-TFET's two-dimensional design. We designed the shape and materials to improve electrostatic control and biosensing capacity. In the proposed device, the conventional gate oxide is replaced with a ferroelectric layer, which plays a crucial role in improving electrostatic control. As a result, due to the negative-capacitance effect, the subthreshold swing is lowered below the theoretical thermal limit of 60 mV/decade at room temperature [27 - 35]. To further address the concern about the leakage, a split-source architecture is used. This configuration has the advantage of suppressing leakage current while increasing band-to-band tunnelling. By strengthening the tunnelling junction at the source-channel interface, the device can generate a faster, more efficient electrical response.

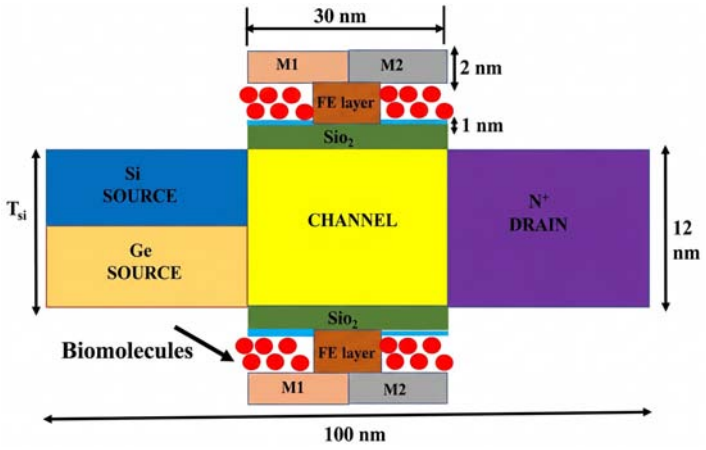

Fig. (1). The construction of the proposed device (FENCB-TFET).

The total device size is kept to 100 nm, and the device layout is based on standard fabrication-compatible protocols owing to the practical feasibility [36]. A thin buffer layer of 1 nm is put between the ferroelectric oxide and the silicon substrate. This layer enhances interfacial stability and reduces lattice mismatch and strain-related effects. During the fabrication process, a thin layer of silicon dioxide (1 nm thick) is deposited and then etched to produce nano-scale cavities at the source and drain regions. These cavities can act as active sensing areas with stable sites for biomolecule immobilisation during sensing operation. Dielectric modulation within these cavities is the basis for the sensing technology. Gate-t--channel coupling affects tunnelling probability and sensitivity as the cavity

CHAPTER 15

Design and Analysis of a Junction-less Double Gate Tunnel Field Effect Transistor (JL-DG-TFET) Based Inverter for Low-Power, High-Performance Digital Circuits

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Abstract: This chapter provides an extensive description of a Junction-less Double Gate-Tunnel Field Effect Transistor (JL-DG-TFET) digital inverter and demonstrates how it outperforms traditional CMOS-based systems. In this inverter, complementary p-type and n-type JL-DG-TFETs are utilized so that better control over leakage current can be achieved, which improves energy efficiency. The JL-DG-TFET is optimized for low power usage, which is achieved due to the steep subthreshold slope, and the absence of junctions further reduces fabrication complexity. SILVACO TCAD and Cadence Virtuoso tools are used for simulations. Simulation results show reduced leakage power, improved noise margin, and minimized average delay. These outcomes illustrate that the JL-DG-TFET-designed inverter is a promising solution for low-power, high-performance circuits and helps address scaling limitations in semiconductor technologies.

Keywords: Boolean-function, Charge plasma, DGTFETs, Junction-less TFETs.

INTRODUCTION

For more than four decades, CMOS technology has been the foundation of digital circuit design, known for its low cost, low power consumption, good performance, reliability, and wide range of applications [1 - 3]. However, as semiconductor technology advances, conventional CMOS devices face serious challenges, including increased leakage current, higher power consumption, and performance limitations [4 - 6]. These challenges primarily arise from the physical limitations of CMOS scaling, which hinder future improvements in energy efficiency and switching speed. For this reason, researchers are actively

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working on alternative transistor technologies to meet the requirements of next-generation digital circuits.

Among available alternative technologies, tunnel field-effect transistors (TFETs) are attracting particular attention because they have the potential to operate below the conventional 60 mV/decade subthreshold limit of MOSFETs.

This characteristic permits the TFET-based devices to improve energy efficiency and reduce overall power consumption [7 - 12]. TFET operates mainly *via* BTBT tunneling, through which charge carriers are transported. Due to BTBT-based transport, we achieve reduced leakage current, improved switching speed, and ultra-low power operation. Due to these properties, TFETs are suitable for miniaturized, energy-efficient electronic devices.

As a significant advancement in TFET technology, a charge-plasma-based junctionless TFET (JL-TFET) has been developed, eliminating the need for a p–n junction [13]. JL-TFET uses a uniform doping profile, which simplifies device fabrication and enables strong electrostatic control. As a result, short-channel effects are reduced, enabling device scaling at the nanometer level [14]. Furthermore, the use of high-k material with an optimized gate work function improves the JL-TFET performance. As a result, precise control over the tunneling barrier is obtai- ned, leading to increased ON-state current and reduced OFF-state current [15].

Material selection plays an important role in optimizing JL-DG-TFET performance. For example, low-band-gap materials such as Ge (germanium) and SiGe, an alloy of Si and Ge, increase the tunnelling probability of the device when added to the source region, thereby increasing device efficiency [16 - 18]. Such an advancement or improvement on JL-DG-TFET makes this device an alternative to CMOS, providing low power dissipation, a simplified device architecture, and better energy efficiency. In this work, an inverter circuit is proposed using complementary n-type and p-type JL-DG-TFETs. The proposed inverter's transistor characteristics are analysed and simulated by SILVACO TCAD, and inverters are analysed by Cadence Virtuoso tools [19]. Our simulation results clearly show that the inverter circuit has a low leakage power, less noise margins, and less delay; therefore, this circuit can be used for future possible solutions.

JL-DG-TFET also has advantages over conventional TFETs, such as the ability to operate at low voltages and to scale devices more effectively while maintaining its characteristics. The steep subthreshold slope of JL-DG-TFETs benefits inverter circuits, which are essential parts of digital electronics. This feature enables the device to operate at lower voltages without sacrificing switching speed, in line with the growing need for high-speed, energy-efficient digital systems.

The rest of the parts are set up in the following order:

- **Part II** delves into the device design and simulation setup, emphasizing the JL-DG-TFET configuration and the tools used.
- **Part III** details the architecture and operation of the inverter, focusing on the complementary use of n-type and p-type JL-DG-TFETs to enhance performance.
- **Section IV** represents and analyzes the simulation outcomes, highlighting improvements in leakage power, noise margins, and delay when compared to conventional designs.

DEVICE DESIGN AND WORKING OF JL-DG-TFET

JL-DG-TFET is made of undoped or mildly doped semiconductor materials, unlike typical transistors, which have strongly doped p-n junctions. This makes the JL-TFET fabrication process easier, improves device uniformity, and promotes device dependability. The absence of abrupt doping changes in the channel region lowers device variability and improves carrier transport.

In JL-TFET, the source and drain regions are also lightly doped or undoped, forming a uniform, continuous doping profile with the channel. This homogeneity minimizes abrupt changes in the electric field, reduces scattering effects, and lowers leakage currents. The gate electrode plays a pivotal role in device functionality by modulating the channel potential and regulating the width of the tunneling barrier. To enhance electrostatic control and reduce dielectric leakage, a high-k dielectric material is placed between the gate electrode and the channel.

Fig. (**1**) illustrates a cross-sectional structure of the Junction-less Dual-Gate TFET (JL-DG-TFET), which may be utilised with both n-type and p-type transistors by simply adjusting the work function of the drain and source. In this configuration, both gates are linked together to increase the ON-state current. To optimise the BTBT process, we utilised a 2 nm SiO_2 gate oxide and a 1 nm HfO_2 high-k dielectric. The simulation parameters for this design are a 50 nm gate length (LG), a 10 nm silicon body thickness (tsi), and a 1.0 V supply voltage (V_{DD}) [13]. In the construction of an n-type DG-TFET, the drain area is created by doping the intrinsic silicon body with electrons at a N^+ concentration, forming the “n” drain. Hafnium, with a work function of 3.9 eV, serves as the drain electrode material. The source region, referred to as the “p” source, is doped with holes at a P+ concentration, and platinum, with a work function of 5.93 eV, is used as the source electrode material. A p-type DG-TFET uses platinum (work function 5.93 eV) as the drain electrode and creates the “p” drain by doping the drain area with

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