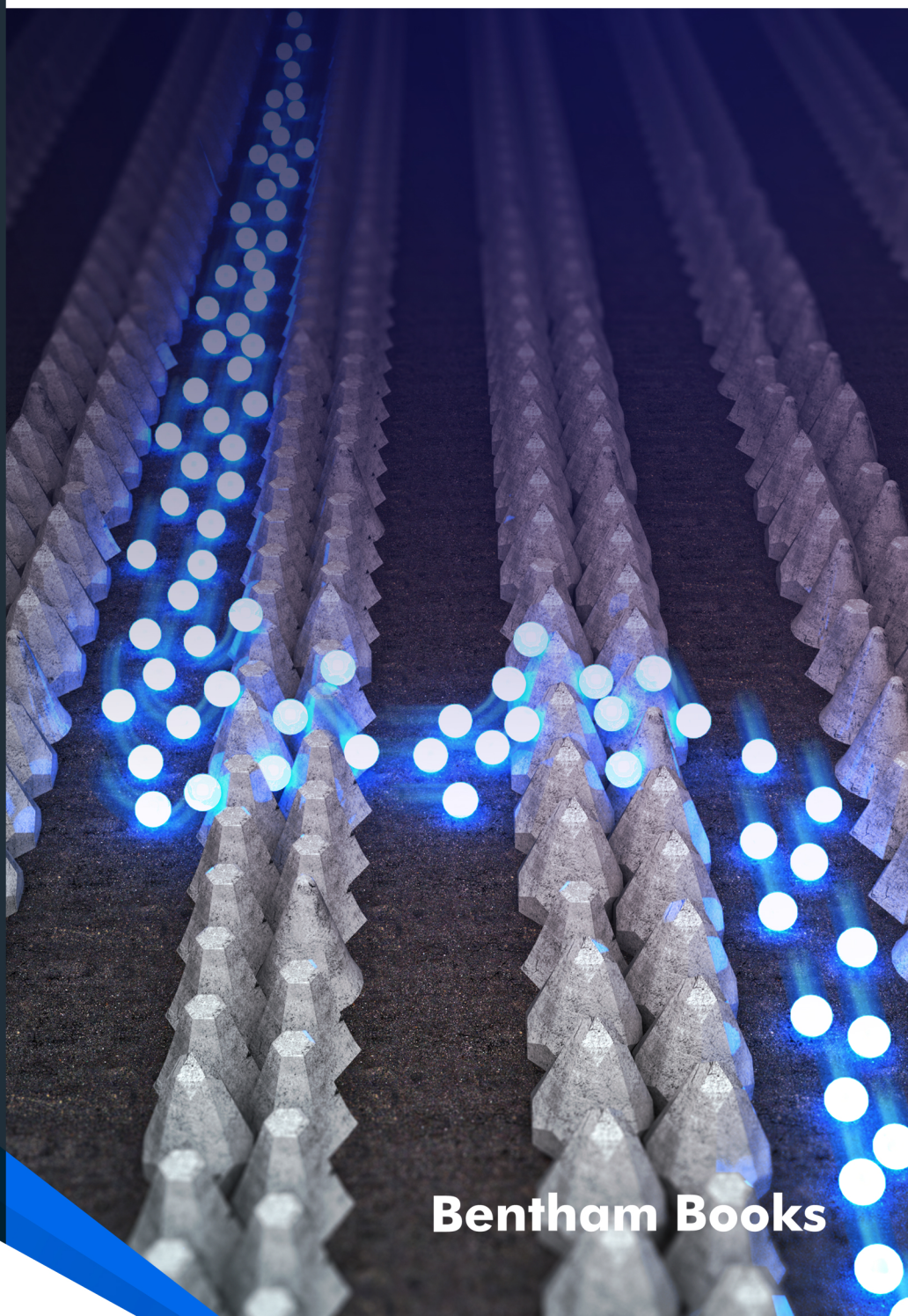
THIN-FILM TRANSISTOR RELIABILITY

Meng Zhang
Mingxiang Wang



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Thin-Film Transistor Reliability

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Thin-Film Transistor Reliability

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FOREWORD

It is with great pleasure that I introduce "Thin-Film Transistor Reliability", a comprehensive exploration into the intricate world of thin-film transistor (TFT) reliability. This book, authored by Prof. Meng Zhang and Prof. Mingxiang Wang, delves deep into the essential aspects of TFT technology, shedding light on the critical factors that influence their reliability. The journey embarked upon in this book takes the reader through a meticulous study of TFTs, from their fundamental principles to the intricate details of reliability analysis methods and stress-induced degradation mechanisms.

The chapters within this book serve as a roadmap guiding readers through the evolution of TFT technology, the various applications in modern electronics, and the challenges posed by environmental factors and stress-induced degradation. By dissecting common defects, exploring reliability analysis techniques, and discussing strategies for improvement, this book equips readers with a comprehensive understanding of TFT reliability.

I commend Prof. Meng Zhang and Prof. Mingxiang Wang for their dedication and expertise in crafting this insightful masterpiece. May this book inspire further exploration and advancements in the realm of TFT reliability, shaping a more robust and reliable future for electronic devices.

Guangcai Yuan
Vice President of BOE Technology Group Co., Ltd.
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PREFACE

Welcome to the exciting world of "Thin-Film Transistor Reliability". This book delves into the intricate details and challenges associated with the reliability of thin-film transistors (TFTs), providing a comprehensive overview of their structure, fabrication processes, and applications in modern electronics. It explores the various degradation mechanisms that affect TFT performance and presents analysis methods to assess their reliability.

Chapter 1 serves as an introduction to TFTs, giving you a solid foundation by discussing their overview, development history, classification, and comparison. It also explores the various applications of TFTs in modern electronics, such as active-matrix displays, sensors, and other circuits. Additionally, this chapter sheds light on the reliability of TFT technology, highlighting the degradation processes that can occur in active-matrix displays, sensors, and other applications. Chapter 2 delves deeper into the reliability issues of TFTs, focusing on the common defects found in silicon-based TFTs and metal oxide TFTs. It explores the different types of defect states and typical degradation mechanisms that affect the performance of TFTs. In Chapter 3, various reliability analysis methods for TFTs are explored. From degradation analysis in different regions to CV curve analysis, low-frequency noise analysis, and thin-film quality analysis, this chapter provides a comprehensive overview of the techniques used to evaluate and analyze the reliability of TFTs. Simulation analysis techniques are also discussed, including TCAD simulation and thermal simulation. Chapter 4 examines the degradation induced by DC voltage stress in TFTs. It covers gate bias stress, hot-carrier effects, and self-heating effects, discussing their impact on both silicon-based TFTs and metal oxide TFTs. Chapter 5 shifts the focus to AC voltage stress-induced degradation in TFTs. It explores the degradation models and behavior of poly-silicon TFTs and metal oxide TFTs under AC stress, highlighting the dependence on waveform elements. A comparison between the two types of TFTs is provided as well. In Chapter 6, circuit-level stress-induced degradation in TFTs is discussed. This chapter covers AC degradation under DC bias, bipolar AC degradation, and ultra-fast AC degradation, shedding light on the impact of different stress conditions on the performance and reliability of TFTs. Chapter 7 explores the effects of environmental factors on TFT reliability. It discusses the influence of temperature, illumination, and moisture on the performance and degradation of TFTs. Finally, Chapter 8 presents strategies and methods for improving the reliability of TFTs. It discusses the implementation of special structures in TFTs and explores other improvement methods, providing valuable

insights into enhancing the overall reliability of these electronic devices. In the concluding chapter, Chapter 9, the key findings and insights presented throughout the book are summarized, providing a comprehensive overview of TFT reliability. The future directions and potential areas of research in the field of TFT reliability are also discussed.

This book aims to provide researchers, engineers, and students with a comprehensive understanding of TFT reliability and the tools to assess and enhance it. It combines theoretical insights with practical knowledge, making it an invaluable resource for anyone involved in the field of electronics. I hope that readers will find this book informative, inspiring, and a catalyst for further advancements in the reliability of TFT.

Finally, we would like to extend our deepest appreciation to our dear students, Mr. Zhendong Jiang, Mr. Guanming Zhu, Mr. Yiming Song, Mr. Yunyang Wang, Mr. Xindi Xu, Ms. Yuwei Zhao, Mr. Pengfei Liu, Mr. Bin Wang, Mr. Qingcan Su, Mr. Zihan Wang, Mr. Feilian Chen, Mr. Mingjun Zhang, Mr. Ruipeng Shen, and Mr. Ming Guo for their invaluable assistance, from collecting research materials to assisting with illustrations and figures. We also would like to express our deep gratitude to the National Natural Science Foundation of China (Grant Number: 62274111) and Shenzhen Municipal Research Program (Grant Number: SGDX20211123145404006) for their generous support throughout the writing process.

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CHAPTER 1

An Overview of Thin-Film Transistors

Abstract. This chapter introduces the fundamental concepts of thin-film transistors (TFTs), outlining their development, classification, and comparison. It delves into the various applications of TFTs in modern electronics, particularly highlighting their role in active-matrix displays, sensors, and other circuits. The chapter also addresses the reliability of TFT technology, focusing on the degradation processes that occur in different applications and the importance of understanding these for the advancement of electronic devices.

Keywords: Application, Development history, Reliability, Thin-film transistors (TFTs).

1.1. INTRODUCTION

Currently, active matrix (AM) display technology is the most mainstream display technology. Thin-film transistors (TFTs), as the core components of AM display technology, greatly influence every aspect of display performance. This chapter will begin with an overview of the development history, classification, and applications of TFTs. It will then provide a detailed discussion of their basic structure, including an introduction to several common types of TFTs, such as polycrystalline silicon (poly-Si) and metal-oxide (MO) TFTs. Following this, the chapter will explore the applications of TFTs in AM displays and extend the discussion to their use in sensors and other areas. The final section will underscore the critical importance of reliability in these various applications.

1.2. OVERVIEW OF THIN-FILM TRANSISTORS

With the rapid development of the Internet of Everything, artificial intelligence, and the 5G era, the electronic information industry has also stepped onto the fast track of soaring development alongside them. Among these advancements, the semiconductor industry's growth has attracted increasing attention. Today, the display FP industry has become an important strategic and foundational industry in the new generation of electronic information fields (Fig. **1**).

Currently, multiple technological pathways are advancing in tandem with innovative technologies springing up rapidly. The established active matrix liquid crystal display (AMLCD) [1, 2] takes the lead, while the high-quality active matrix organic light emitting diode (AMOLED) [3] serves as a premium technological

successor. Additionally, micro light emitting diodes (Micro-LEDs) [4], laser projections, and electronic paper are expanding the display realm for specific applications. The domain of display technology has progressively moved beyond conventional settings like televisions, mobile devices, and surveillance systems to encompass areas such as smart homes, educational technology, community smart systems (Fig. **2**), autonomous vehicles, remote healthcare, virtual reality, and augmented reality.

Fig. (1.1). Displays in mobile phones, tablets, and computers.

TFTs are electronic components extensively applied in the realm of display technology, commonly utilized as switches to regulate current flow. Serving as the cornerstone of AM driving systems, TFTs are essential in both pixel arrays [5] and driving circuits [6], exerting a profound influence on the quality and manufacturing efficiency of display devices. Their structure, manufacturing processes, characteristics, and reliability are critical to the performance of displays. Therefore, research into TFTs has become a focal point in the field of display technology.

1.2.1. The Development History of Thin-Film Transistors

The origins of TFT development can be traced back to 1925 when Julius Edgar Lilienfeld (Fig. **3**) innovatively proposed the concept of the effect transistor (FET) and applied for a patent for the FET invention five years later [7]. However, due to the limitations of the theories and conditions at the time, Lilienfeld did not recognize that the active layer in an FET must be made of semiconductor materials.

It wasn't until 1935 that Heil explicitly proposed the crucial theory that the active layer of an FET must be made of semiconductor materials [7]. However, the requirements for the electronic manufacturing process in solid-state devices greatly exceeded the capabilities of the production techniques available at that time, preventing the concept from advancing beyond the theoretical stage and resulting

in no finished devices being produced. It was not until the 1950s that the production of FETs truly became a reality. The world's first junction, FET, was proposed by Shockley (Fig. **4**) in 1952 and successfully fabricated by Dacey and others in 1954 [8].

Fig. (1.2). Data visualization display in smart communities.

Fig. (1.3). Julius Edgar Lilienfeld (1882.4.18-1963.8.28).

CHAPTER 2

Overview of Reliability Issues in Thin-Film Transistors

Abstract. This chapter provides an in-depth analysis of the reliability issues associated with thin-film transistors (TFTs), focusing on the common defects found in silicon-based and metal-oxide TFTs. It discusses the various types of defect states and the typical degradation mechanisms that impact the performance of TFTs. The chapter emphasizes the need for comprehensive understanding and strategies to mitigate these reliability challenges in TFT applications.

Keywords: Defect states, Degradation mechanisms**,** Metal oxide TFTs, Reliability, Silicon-based TFTs.

2.1. INTRODUCTION

The reliability of thin-film transistors (TFTs) is a critical determinant of their practical application. Thus, an analysis of TFT reliability is imperative. Unlike metal-oxide-semiconductor (MOS) devices, TFTs contain a significant number of defects. The reliability issues of TFTs often stem from the various defect states within the device. Therefore, understanding the defect state density within the device and its impact on performance is fundamental for subsequent reliability analysis.

In this chapter, we delineate common defect state densities found in silicon-based and metal-oxide (MO) TFTs, along with their effects on device performance. Building on this foundation, we also introduce several common classification methods for defect states and discuss the impact of different types of defect states on device performance. Lastly, we briefly outline several typical degradation mechanisms in TFTs.

For TFT to meet the requirements of actual production, characterizing the fundamental performance of the devices is a crucial initial step. The *I-V* (current-voltage) characteristics of TFTs can primarily be categorized into output characteristics and transfer characteristics, as shown in Fig. (**2.1**). Typically, the output characteristics of a device are measured by fixing the gate voltage and varying the drain voltage, while the transfer characteristics are obtained by fixing the drain voltage and varying the gate voltage. Commonly, the drain voltage is set

to 0.1 V and 5 V (or their negative equivalents) depending on the polarity of the TFT's active layer to represent the device's performance in linear and saturation conditions, respectively. When testing the organic TFTs, the drain voltage can be set to a larger level.

2.2. BASIC PERFORMANCE CHARACTERIZATION OF THIN-FILM TRANSISTORS

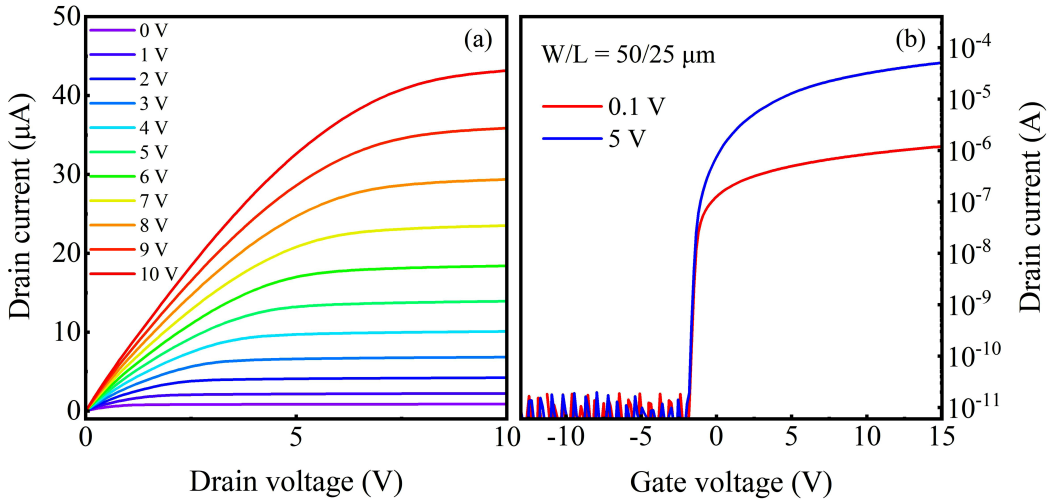

Fig. (2.1). (a) Output_characteristic curve and (b) transfer characteristic curve of a typical TFT.

By analyzing the IV curves of TFTs, numerous key fundamental performance characteristics of the devices can be extracted:

(1) Mobility (μ)

Mobility is a key indicator of device performance, defined as the average drift velocity of charge carriers under the influence of a unit electric field. It reflects the ease with which charge carriers drift in response to an external electric field, with units of m^2/Vs or cm^2/Vs. The magnitude of mobility is primarily related to scattering within the device, such as lattice scattering and ionized impurity scattering. Unlike MOS devices, TFTs have a significant number of defect states within the bulk of their active layers, which can capture charge carriers during their motion. Therefore, the density of defect states in the TFT's active layer directly affects its mobility [1, 2]. Mobility can be simply derived from the linear region of the TFT's transfer characteristic curve using the following formula [3]:

$$\mu = g_m \cdot \frac{L}{W \cdot C_{ox} \cdot V_{ds}} \quad \textbf{(2.1)}$$

Where g_m is the maximum transconductance of the TFT, which can be obtained from the slope of the transfer characteristic curve. Besides, the saturation mobility can be simply derived from the saturation region of the TFT's transfer characteristic curve using the following formula:

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_D}}{dV_G}\right)^2}{\frac{1}{2}C_{OX}\frac{W}{L}} \quad \textbf{(2.2)}$$

Generally, increasing temperature can enhance carrier thermal motion [4], thus increasing mobility, but excessively high temperatures may also lead to an increase in lattice defects, which can reduce mobility [5-7]. Electric fields also affect carrier mobility; for example, devices can experience mobility degradation under negative/positive bias temperature instability (PBTI/NBTI) stress [8, 9] and negative/positive bias illumination stress (NBIS/PBIS) conditions [10].

(2) Threshold Voltage (V_{th})

The V_{th} in metal-oxide-semiconductor field-effect transistors (MOSFETs) typically refers to the gate voltage required for the device to just enter strong inversion. TFTs, on the other hand, usually operate in the accumulation region. Thus, the V_{th} for a TFT indicates the gate voltage at which charge carriers begin to accumulate in the channel. There are two common methods for extracting V_{th}. The first method is based on the fundamental definition of V_{th}, which identifies it as the gate voltage corresponding to a certain drain current level, typically defined as [11]:

$$V_{th} = V_{gs}(I_{th} = 1nA, V_{ds} = 0.1V) \quad \textbf{(2.3)}$$

$$V_{th} = V_{gs}(I_{th} = 10nA, V_{ds} = 5V) \quad \textbf{(2.4)}$$

The second method involves extracting the on-state region of the transfer characteristic curve in linear coordinates [12], extending the linear portion backward to intersect the horizontal axis, and defining the corresponding voltage value as V_{th}. Factors such as semiconductor material properties [13], insulator thickness [14], gate structure [13], temperature [5, 15, 16], light exposure [17-20],

CHAPTER 3

Reliability Analysis Methods for Thin-Film Transistors

Abstract. This chapter explores the various methods used for reliability analysis of Thin-Film Transistors (TFTs). It covers transfer curve degradation analysis techniques, capacitance-voltage curve analysis, low-frequency noise analysis, and thin-film quality assessment. Additionally, the chapter discusses simulation analysis methods, including TCAD simulation and thermal simulation, which are crucial for evaluating and enhancing the reliability of TFTs in electronic applications.

Keywords: CV curve analysis, Low-frequency noise analysis, Reliability analysis methods, Simulation analysis.

3.1. INTRODUCTION

Thin-film transistors (TFTs) can be characterized by a variety of performance measurements, each with its strengths and weaknesses due to different emphases. For reliability analysis of TFTs, different characterizations must be employed based on the specific degradation phenomena and mechanisms.

This chapter presents the measurement and analysis methods for basic transfer characteristic curves, output characteristic curves, and capacitance-voltage characteristic curves. It then delves into the analysis methods for low-frequency noise and several quality assessment techniques for devices. Finally, it introduces two commonly used simulation approaches for semiconductor devices: device simulation and thermal simulation.

3.2. BASIC TRANSFER CURVE DEGRADATION ANALYSIS

3.2.1. Degradation in On-State Region

The on-state region of a thin-film transistor (TFT) device typically begins after the device's threshold voltage (V_{th}) [1]. In logarithmic coordinates, it is usually located in the region where the current growth flattens for large gate voltages, as shown in Fig. (**3.1**). As stated in section 2.1, the current at a fixed gate voltage can generally be considered the on-state current (I_{on}).

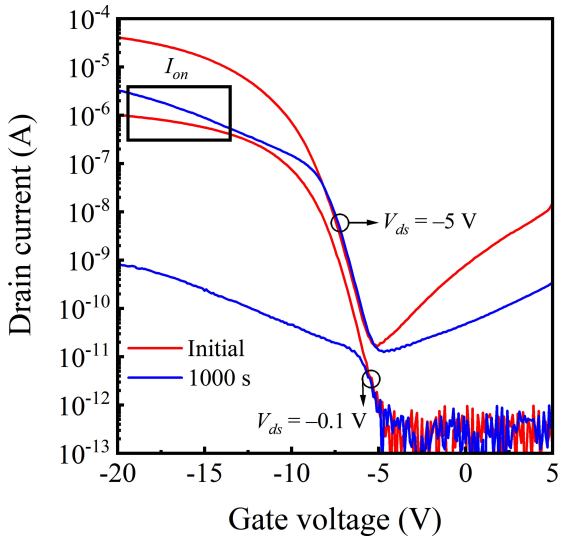

Fig. (3.1). The on-state region of a TFT device and its degradation.

Various stresses typically affect the device's I_{on}, which often experiences significant degradation, such as that caused by hot carrier (HC) stress. Defects that cause I_{on} degradation are usually tail states, which is due to their higher density and closer proximity to the conduction or valence bands, making them more likely to capture free charge carriers [2]. In reliability analysis, the change rate of I_{on} (ΔI_{on}) is commonly used to assess the reliability of the device in the on-state, expressed by the following equation [3]:

$$\Delta I_{on} = \frac{I_{on}(stress) - I_{on}(initial)}{I_{on}(initial)} \quad \textbf{(3.1)}$$

However, there can be some issues in determining the I_{on} using the fixed voltage method. For instance, when threshold voltage (V_{th}) shifts significantly, the I_{on} will correspondingly increase or decrease. However, this type of I_{on} degradation is usually not caused by tail-state defects. To express the I_{on} more accurately, the following formula can be used [4]:

$$I_{on} = I_d(V_{th} + 6\ V) \quad \textbf{(3.2)}$$

This method can effectively eliminate the impact of V_{th} shift on I_{on}. However, the I_{on} only provides a rough indication of the overall device performance. The true cause of device degradation requires further analysis using other methods.

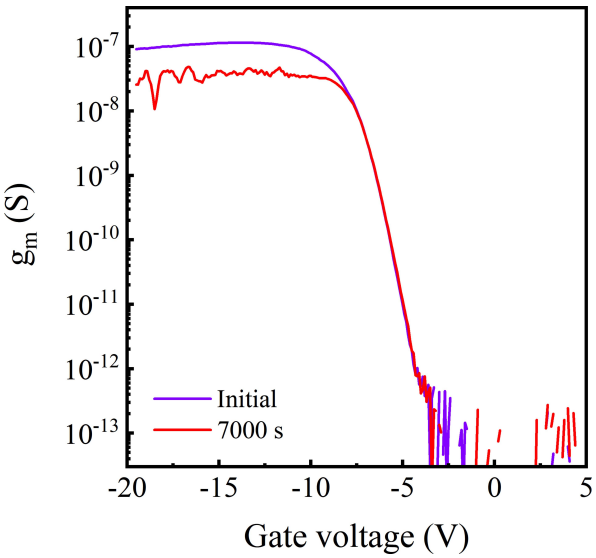

Fig. (3.2). Variation of g_m with V_g voltage for TFT device.

In addition, the mobility of a device can be extracted in the on-state region, as shown in Fig. (**3.2**). The magnitude of the device's mobility is directly related to the scattering within the active layer of the device. It can be represented by the following formula [5]:

$$\frac{1}{\mu} = \frac{1}{\mu_i} + \frac{1}{\mu_s} + \frac{1}{\mu_0} \tag{3.3}$$

Here, μ_i represents acoustic phonon scattering, μ_s represents ionized impurity scattering, and μ_0 represents optical phonon scattering [6]. Typically, during various types of degradation, the increase in various types of defect states can significantly enhance ionized impurity scattering or other types of scattering. This leads to a noticeable decrease in the device's mobility, which in turn contributes to further degradation in the on-state region of the device.

3.2.2. Degradation in Subthreshold Region

The subthreshold region of a device is a critical area affecting its operational performance, typically representing when the device turns on and how quickly it does so. Two main factors are generally studied in this region: the V_{th} and the subthreshold swing (*SS*), both of which degrade differently from phenomena observed in the on-state region [7, 8].

CHAPTER 4

Direct Current Voltage Stress-Induced Degradation in Thin-Film Transistors

Abstract. This chapter investigates the degradation induced by direct current（DC）voltage stress in thin-film transistors (TFTs). It provides a detailed examination of gate bias stress, hot-carrier effect, and self-heating effect, discussing their impact on silicon-based and metal oxide TFTs. The chapter aims to summarize and analyze the influence of these degradation mechanisms on the performance and reliability of TFT devices.

Keywords: DC voltage stress, Hot-carrier effect, Metal oxide TFT, Self-heating effect, Silicon-based TFT.

4.1. INTRODUCTION

In the context of thin-film transistor (TFT) reliability research, it is essential to consider the electrical reliability of TFTs, as these devices are inevitably subjected to various voltage conditions during operation. The study of TFT electrical reliability is both fundamental and widespread, focusing on the examination of device degradation under long-term application of electrical stress and the observation of the resulting degradation phenomena.

TFT electrical reliability can be categorized into two main types: direct current (DC) electrical stress reliability and alternating current (AC) electrical stress reliability. Research on DC electrical stress reliability forms the foundation of reliability studies involving the application of prolonged DC stress to the gate and drain electrodes of TFTs and monitoring the subsequent degradation. Different stress application methods can lead to various degradation scenarios, such as on-state current (I_{on}) degradation or subthreshold swing (SS) degradation. Therefore, to address TFT reliability issues, it is necessary to conduct targeted research into the physical mechanisms behind different degradation phenomena and to modify device structures or alter stress application methods to suppress device degradation.

Typically, degradation due to DC electrical stress reliability can be classified into several types: gate DC bias stress degradation, hot carrier (HC) degradation, and self-heating (SH) degradation. Gate DC bias stress degradation primarily encompasses both positive bias stress (PBS) and negative gate bias (NBS) degradation. This chapter will provide a summary and analysis of the impact of the

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aforementioned three degradation mechanisms on silicon-based and metal oxide (MO) TFT devices.

4.2. GATE BIAS STRESS

In operation, the gate electrode of a TFT serves as the primary control element for modulating the device's on-off state and is typically subjected to various prolonged voltage stresses. Consequently, gate bias stress is often the most fundamental area of TFT reliability research. The standard method of applying stress involves imposing a long-duration gate bias while grounding the source electrode and drain electrode. Regardless of the biasing condition, either PBS or NBS, the most common degradation phenomenon is a shift in the threshold voltage (V_{th}). Typically, devices exhibit a positive shift under PBS [1-13] and a negative shift under NBS [1, 2, 4, 7, 14-22]. The mainstream explanation for gate bias stress involves carrier trapping at the interface or within the gate insulator (GI), where a high concentration of charged particles can shield the electric field of the gate, leading to premature or delayed device turn-on [4-6, 12, 14, 15].

However, the aforementioned mechanism alone cannot fully explain the entire range of degradation phenomena observed in TFTs under both PBS and NBS, especially for MO TFTs. In addition to the expected positive threshold voltage (V_{th}) shift during PBS [8, 9], some MO TFTs have exhibited a negative V_{th} shift [22]. Concurrently, the wide bandgap of MO TFTs makes it difficult to ionize holes directly under NBS. Therefore, a multitude of alternative explanations for gate bias stress degradation coexist alongside the mainstream mechanism [2, 21].

4.2.1 Positive Bias Stress

As previously mentioned in session xxx, PBS is typically characterized by the imposition of a positive voltage bias on the gate terminal of a transistor. Different types of TFT devices exhibit varying degradation phenomena and mechanisms under PBS. This section primarily discusses the PBS degradation of two types of TFT devices: silicon-based (Si-based) TFTs [1-3, 13] and MO TFTs [4-9, 12], which will be introduced separately in the following content.

4.2.1.1. Positive-Bias-Stress-Induced Degradation in Silicon-Based Thin-Film Transistor

After polycrystalline silicon (poly-Si) TFTs are subjected to PBS stress, the degradation is typically not pronounced, with the primary manifestation being a shift in the V_{th} [1]. The V_{th} shift is mainly due to electron injection into the GI layer,

as previously discussed, which creates fixed charges. These fixed charges shield the electric field, leading to premature or delayed device turn-on and resulting in V_{th} shift. As mentioned in Chapter 2, degradation in *SS* and I_{on} is generally related to the generation of defect states. However, for poly-Si TFTs, the channel and interface do not have as many weak bonds, and PBS generally does not produce defect states or only a small number that are insufficient to cause *SS* and I_{on} degradation. Poly-Si TFTs typically require a larger bias voltage to exhibit significant degradation [2], which is usually analyzed in combination with additional conditions such as temperature or light exposure for reliability assessment [2].

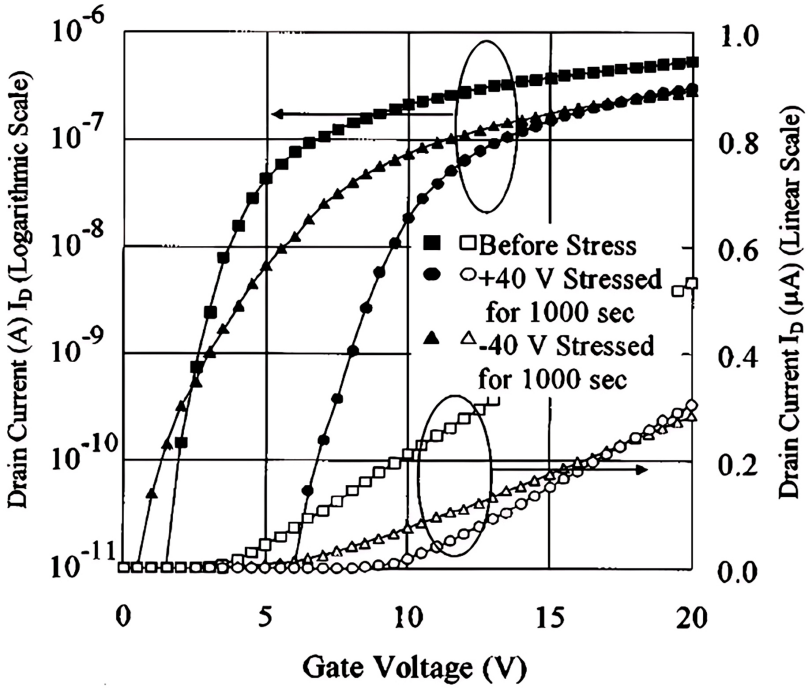

Fig. (4.1). Degradation of a typical a-Si:H TFT device under PBS and NBS stresses [1].

Thin-film transistors fabricated from hydrogenated amorphous silicon (a-Si:H) utilize silicon nitride as the GI and show different PBS reliability characteristics. Under PBS, in addition to a positive shift in V_{th}, there is also degradation in *SS* and I_{on}. Fig (**4.1**) displays the shift in the transfer characteristics of an a-Si:H thin-film transistor when subjected to a gate voltage stress for 1000 seconds, as observed at a constant drain voltage of 1 V, both pre- and post-stress application. It is evident that after a 40 V PBS stress, the device exhibits a significant positive shift in V_{th}, along with a noticeable change in *SS*, deviating notably from the typical response

CHAPTER 5

Alternating Current Voltage Stress-Induced Degradation in Thin-Film Transistors

Abstract. This chapter investigates the degradation induced by alternating current (AC) voltage stress in thin-film transistors (TFTs). It provides a detailed examination of AC voltage stress, discussing its impact on silicon-based TFTs and metal oxide TFTs. The chapter aims to summarize and analyze the influence of these degradation mechanisms on the performance and reliability of TFT devices.

Keywords: Alternating current (AC), AC hot carrier (HC) effect, Degradation models, Metal oxide TFTs, Polycrystalline silicon TFTs, Waveform elements.

5.1. INTRODUCTION

Chapter 4 provided a detailed discussion on the degradation of thin-film transistors (TFTs) under direct current (DC) stress. However, as mentioned in Section 1.4.1, the actual operating state of a TFT is subject to a superposition of various changing signals. Therefore, the study of alternating current (AC) reliability is more aligned with the actual working conditions of TFTs compared to DC reliability research.

Current research methods for investigating the AC reliability of TFTs primarily involve applying periodic pulse stress to either the gate or the drain and observing the resulting degradation in the device. For Si-based TFTs, the application of AC stress typically leads to changes in the device's on-state current (I_{on}), while for metal oxide (MO) TFTs, AC stress usually results in a shift in the device's threshold voltage (V_{th}).

The mechanisms proposed to explain the above degradation phenomena largely focus on the AC hot carrier (HC) effect. Under the application of AC stress, a large number of HCs are generated within the device due to the influence of a strong electric field, leading to device degradation. This chapter presents the degradation conditions of Si-based TFTs and MO TFTs under single-ended AC stress and the related degradation mechanism.

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5.2. ALTERNATING CURRENT DEGRADATION MODEL IN POLYCRYSTALLINE THIN-FILM TRANSISTORS

5.2.1. Degradation Behavior of Polycrystalline Thin-Film Transistors under Alternating Current Stress

As illustrated in Fig. (**5.1**), the degradation of the transfer characteristics of a polycrystalline silicon (poly-Si) TFT under AC gate stress is shown for different drain voltages of –0.1 V and –5 V. The AC stress conditions were applied with a rising time (t_r) of 1 ns, a falling time (t_f) of 50 ns, a duty cycle of 50%, a peak voltage (V_{peak}) of 10 V, and a base voltage (V_{base}) of –10 V. It is evident that the device exhibits clear signs of HC degradation, characterized by a significant reduction in I_{on}, while the subthreshold region remains largely unchanged.

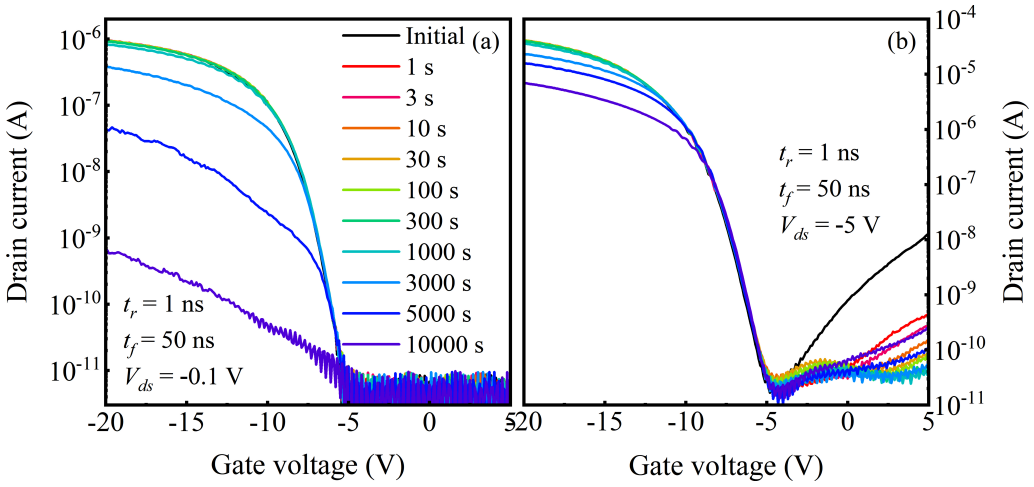

Fig. (5.1). Transfer characteristic curves with time under V_g stress for V_{ds} of –0.1 V and 5 V.

Upon comparing the transfer characteristics curves at different drain-source voltage (V_{ds}), it is apparent that the degree of degradation at –5 V is notably less than that at –0.1 V. Moreover, the device at –5 V shows a distinct phenomenon of degradation followed by an increase in the off-state current (I_{off}). These degradation phenomena are typical for poly-Si TFTs, and the extent of degradation can vary depending on the conditions of the applied AC stress [1].

5.2.2. Waveform Elements Dependence of Alternating-Current Degradation

Fig. (**5.2**) typically illustrates the pulse stress applied to TFTs [1], which can be categorized based on the location of application into AC gate stress [1-10] and AC

drain stress [11-14]. Depending on the pulse shape, pulse stress can generally be divided into several components: t_r、t_f、peak time (t_{peak})、base time (t_{base})、and V_{peak} and V_{base} [1-14].

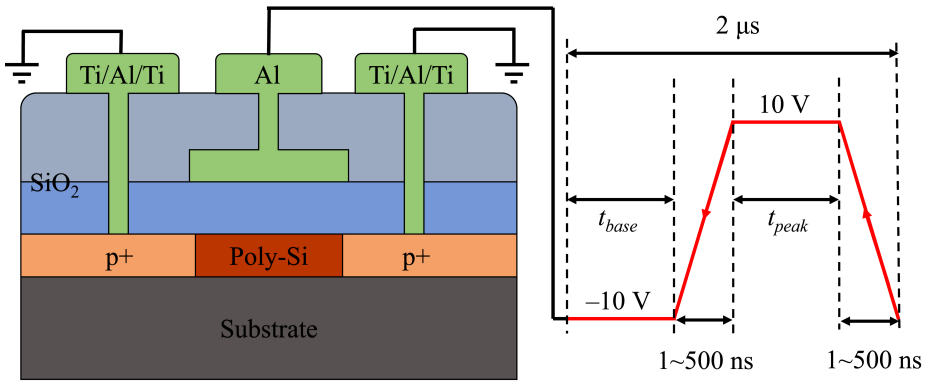

Fig. (5.2). The schematic diagram of poly-Si TFTs and the waveform of the gate voltage pulse [1].

Usually, the degradation caused by gate and drain pulse stresses are similar, but gate stress often results in less degradation due to the blocking effect of the gate insulator (GI) layer under the same voltage conditions. Variations in these pulse conditions can influence the extent of device degradation to a certain degree.

5.2.2.1. Peak Voltage and Base Voltage

As two critical parameters that determine the pulse amplitude, the magnitude of V_{peak} and V_{base} will directly affect the degradation of TFTs under AC stress. The difference between V_{peak} and V_{base}, *i.e.*, the pulse amplitude, will cause greater I_{on} degradation when larger, provided all other conditions are equal. As shown in Fig (**5.3**), for a fixed V_{base} of 0 V and varying V_{peak}, the decay is intensified with an increased pulse magnitude. Across various amplitudes, a uniform degradation gradient of 1.0 is consistently noted, indicat

ing the potential involvement of a reaction-limited mechanism for defect generation. If the scale of the ordinate is altered, it can be seen that the device experiences a region of initial I_{on} increase, with larger voltage amplitudes leading to higher increases in I_{on}, although these increases decline more rapidly [4, 11].

CHAPTER 6

Circuit-Level Stress-Induced Degradation in Thin-Film Transistors

Abstract. This chapter discusses the degradation of Thin-Film Transistors (TFTs) under circuit-level stress, which is crucial for understanding their performance and reliability in practical applications. It covers AC degradation under DC bias, bipolar AC degradation, and ultra-fast AC degradation, providing insights into the impact of different stress conditions on the TFTs' performance and reliability.

Keywords: AC degradation, Bipolar AC degradation, Circuit-level stress, DC bias, Performance, Reliability, Ultra-fast AC degradation.

6.1. INTRODUCTION

Chapter 5 provided a detailed discussion on the degradation of thin-film transistors (TFT) under alternating current (AC) stress and its causes, with the non-equilibrium PN junction model effectively explaining the basic degradation patterns. However, Chapter 5 primarily focused on the degradation under single-ended AC stress. In the actual operating state of TFTs, multiple electrodes of the device are simultaneously exposed to various stress conditions. As mentioned in Section 1.4.1, a switch TFT may be exposed to an AC state at the gate and drain simultaneously or a direct current (DC) state at the gate with an AC state at the drain; for a driver TFT, the drain is typically connected to V_{DD} for extended periods, while the gate is directly exposed to various AC environments.

Therefore, based on the actual working conditions of TFTs, the degradation of TFTs can be categorized into AC stress reliability under DC bias and dual-end AC stress reliability.

With the current pursuit of high refresh rates and high-resolution displays, TFTs will be exposed to increasingly faster AC frequencies, transitioning from the μs range to the ns range. Consequently, to reflect the actual working conditions of TFTs more accurately, further research is needed on the degradation of TFTs under faster pulse stress.

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6.2. ALTERNATING CURRENT DEGRADATION UNDER DIRECT CURRENT BIAS

This section primarily examines the degradation phenomena and mechanisms of TFT devices when one end is subjected to AC stress while the other end is under DC bias [1-4]. This mode of stress is more aligned with the actual forces exerted on devices in real-world scenarios and is better suited for circuit-level reliability studies. Consequently, an understanding of the fundamental Active Matrix Organic Light Emitting Diode (AMOLED) circuitry is required. An AMOLED display circuit typically comprises two TFTs and a capacitor [5-7]. In practical applications, both the gate and drain of these two TFTs are subjected to complex stresses. For instance, they may experience simultaneous AC stress [8-11], or one end may be under AC stress while the other end is under DC stress [1-4], as depicted in Fig. (**6.1b**). Therefore, studying the degradation of TFT devices under stress at both ends is essential. The stress conditions illustrated in Fig. (**6.1c**) are designed to simulate the stresses encountered by TFTs in real-world applications.

The condition for driving stress [1, 2] is that the gate terminal of the TFT is subjected to an AC voltage of positive and negative 11.5 V in magnitude, with adjustable rise time, high-level duration, fall time, and low-level duration. At the same time, the source terminal of the TFT is subjected to a positive DC voltage, as shown in Fig. (**6.1c**). Furthermore, in an alternative experimental setup, a DC voltage is applied to the gate terminal of the TFT, while an AC voltage, oscillating between positive and negative 10 V, is imposed on the drain terminal. This configuration, illustrated in Fig. (**6.1d**), is known as"OFF-state stress."

The performance deterioration of polycrystalline silicon (poly-Si) TFTs under the described "driving" stress is examined and characterized. It is evident that this type of stress-induced degradation is mainly attributed to a dynamic hot carrier (HC) effect. The severity of the degradation is exacerbated by a shorter t_r, leading to more pronounced dynamic HC effects.

Furthermore, the analysis of poly-Si TFTs under OFF-state stress conditions [3, 4] indicates that the degradation is chiefly governed by the dynamic HC effect. This effect is predominantly determined by the pulse t_f and appears to be largely unaffected by the pulse t_r.

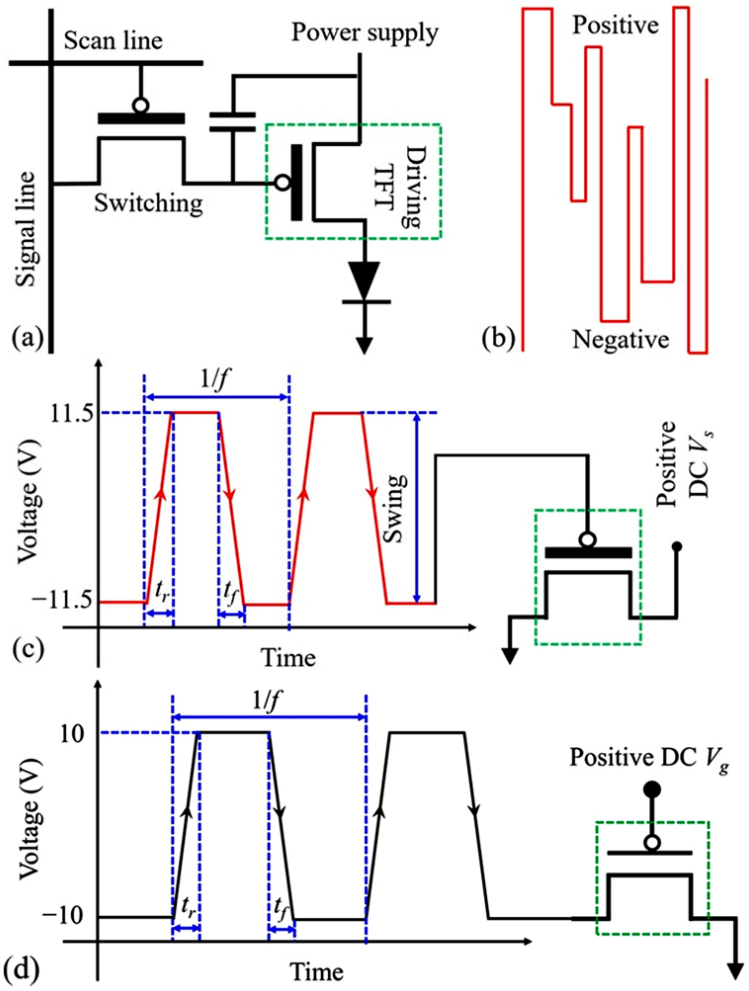

Fig. (6.1). (a) Schematic of 2T1C circuit of a pixel in an AMOLED display. (b) Practical voltage pattern applied to the gate electrode of the driving TFT. (c) "Driving" stress conditions for a driving TFT. (d) OFF-state stress conditions for a switching TFT [2, 4].

6.2.1. "Driving"-Stress-Induced Degradation

Fig. (**6.2a**) illustrates the temporal evolution of the transfer characteristics in a conventional poly-Si TFT under "driving" stress. This stress condition is characterized by an AC gate stress superimposed on a DC V_s of 10 V. Observations indicate that both the I_{on} and gate-induced drain leakage (GIDL) current [12] experience a continuous decline with increasing stress duration, while the subthreshold swing (*SS*) remains relatively unaffected. Additionally, a recovery in

CHAPTER 7

Environmental Stress-Induced Degradation in Thin-Film Transistors

Abstract. This chapter explores the impact of environmental factors on the reliability of thin-film transistors (TFTs), discussing the effects of temperature, illumination, and moisture on the performance and degradation of TFTs. It provides a comprehensive analysis of how these environmental conditions can influence the overall reliability and stability of electronic devices incorporating TFTs.

Keywords: Degradation, Environmental reliability, Illumination, Moisture, Temperature, TFT performance.

7.1. INTRODUCTION

In addition to electrical stress reliability, thin-film transistors (TFT) are often subject to various environmental factors such as temperature, humidity, and light exposure. Under the combined influence of electrical stress and environmental conditions, the degradation of devices may be suppressed or enhanced to varying degrees, and even new types of degradation mechanisms may emerge. Research into this type of degradation is typically more complex, requiring consideration of both the changes within the device caused by electrical stress, such as internal electric fields and current, as well as the impact of environmental factors on carrier movement, generation, and recombination. Moreover, the effects of certain environments, like humidity, may lead to additional and distinct degradation phenomena that necessitate separate investigation.

To study the impact of these environmental factors, researchers often examine the degradation of devices under the simultaneous influence of electrical stress and environmental conditions, probing the underlying degradation mechanisms. In this work, we focus on the degradation of silicon-based (Si-based) TFTs and metal oxide (MO) TFTs under various stress conditions induced by temperature, light exposure, and humidity.

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7.2. EFFECTS OF TEMPERATURE ON THIN-FILM TRANSISTORS RELIABILITY

7.2.1. Effect of Temperature on the Reliability of Polycrystalline Silicon Thin-Film Transistors

As one of the most mainstream types of TFT devices, polycrystalline silicon (poly-Si) TFTs boast advantages such as high mobility and reliability. Since TFTs primarily operate in environments with complex electrical signals and are subject to temperature interference affecting reliability, research on TFT reliability has mainly focused on the electrical aspects, with temperature's impact on device performance studied across various electrical reliability scenarios.

Common degradation mechanisms affecting poly-Si TFT reliability include self-heating (SH), hot carrier (HC) effects, and positive/negative bias temperature instability (PBTI/NBTI). These are summarized for n-type poly-Si TFTs in Table **1**. We will now delve into these degradation mechanisms in more detail.

Table 1. Relationship between common degradation phenomena and temperature in poly-si TFT.

Degradation model	Gate voltage (V_g)	Drain voltage (V_d)	Temperature (T)
Self-heating	Large	Large	Worse as the temperature rises
Hot carrier	Slightly larger than V_{th}	Large	Worse as the temperature decreases
NBTI	Large	Ground	Worse as the temperature rises

(a) The Impact of Temperature on Poly-Si TFT Self-Heating Effects

SH degradation is generally believed to be caused by Joule heat from the on-state current (I_{on}), which raises the device temperature. Since the I_{on} is proportional to W/L, the heat power generated $P = I_{on} \cdot V_{ds}$ is also proportional to W/L. For devices with equal W/L ratios, small-sized devices generate more heat per unit area and have less heat dissipation area. Consequently, SH is more pronounced in smaller devices with larger W/L ratios. Satoshi Inoue and colleagues used an infrared thermometer to measure the surface temperature of devices with different dimensions under the same V_g and V_d electrical stress. They found that for a W/L of 100 μm/100 μm, the temperature was 70.6 °C, for 10 μm/10 μm, it was 104.6

°C, and for 100 μm/10 μm, it was 215.5 °C. For devices with the same channel length, as the channel width increases under the same V_g and V_d stress, the degradation of threshold voltage (V_{th}) becomes more severe. In experiments with devices in parallel, they also found that degradation was not uniformly distributed along the channel, with the center degrading more than the edges, similar to the non-uniform temperature distribution within the channel [1]. This indicates that device degradation is related to its temperature.

It is commonly accepted that Si-H bonds break down above 350 °C, so when the device temperature is high, many dangling bonds are formed at the Si/SiO_2 interface, increasing the interface state density and causing device performance degradation. Satoshi Inoue and colleagues confirmed this through two-dimensional device simulations using Atlas software, where increasing the state density in the channel region yielded results consistent with experimental data [2]. Mutsumi Kimura and colleagues' research on the interface and channel defect density in poly-Si TFTs also showed that SH degradation is due to the increase in interface state density caused by Si-H bond breakage at the Si/SiO_2 interface, with a slight increase in defect density at the grain boundaries in the channel [3]. This confirms that the generation of SH is indeed related to the Joule heat produced by the current during device operation and becomes more severe with increased environmental temperature.

(b) The Impact of Temperature on Poly-Si TFT Hot Carrier Effects

HC degradation typically occurs when devices, during operation, generate HCs due to the large electric field near the drain, leading to impact ionization and damage to the interface and channel lattice near the drain, increasing the trap state and causing device performance degradation [2, 4-13]. This is mainly manifested in the transfer curve as a decrease in I_{on} and an increase in off-state current (I_{off}), while V_{th} and subthreshold swing (SS) usually do not change significantly. This is because HC damage typically occurs near the drain, so it has a minimal impact on V_{th} and SS, which are related to the overall channel properties. This was confirmed by Toshiyuki Yoshida and colleagues [7]. They performed charge pump (CP) experiments on devices and found minimal changes in CP current, indicating little change in interface traps within the channel.

HC effects are most pronounced when V_d is large and the gate voltage is slightly above V_{th}. A large V_d significantly shields the longitudinal electric field near the drain, reducing the carriers near the drain and causing the device to "pinch off." At this point, the electric field generated by the large V_d mainly falls on the pinch-off

CHAPTER 8

Strategies for Improving Thin-Film Transistor Reliability

Abstract. This chapter presents strategies for enhancing the reliability of thin-film transistors (TFTs), discussing the implementation of special structures and other improvement methods. This chapter focuses on the reliability improvement of polysilicon TFT in lightly doped drain (LDD) and bridge-grain (BG) structures. The method to improve the reliability of metal oxide TFT is also described, such as the elevated-metal metal oxide (EMMO) structure.

Keywords: Bridge-grain (BG), Elevated-metal metal oxide (EMMO), Lightly doped drain (LDD), Reliability improvement strategies.

8.1. INTRODUCTION

The previous chapters of this book have detailed the reliability variations of thin-film transistors (TFT) under different operating conditions and the various degrees of damage caused by the application of multiple stresses. If such damage occurs directly within the display, it will lead to a degradation of the display's overall performance. Furthermore, as devices are typically integrated within systems, this decline in overall performance is challenging to remedy.

To address the different types of degradation encountered in devices, it is necessary to improve their reliability in a targeted manner. Based on the common causes of degradation, methods to enhance the reliability of devices can generally be categorized into adjusting the signal voltage levels or modifying the TFT devices themselves. However, adjusting signal sizes can impact the overall performance of the display to some extent, especially in circuit design aspects. Therefore, improving device reliability often requires adjustments to the devices themselves. This chapter focuses on two typical structures: the lightly doped drain (LDD) structure and the bridged grain (BG) structure. Both of these structures can significantly enhance the inherent reliability of TFTs. The chapter also introduces additional methods for improving device reliability.

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8.2. LIGHTLY DOPED DRAIN STRUCTURE IN THIN-FILM TRANSISTORS

In the pursuit of continually improving device performance and increasing the number of devices per unit area, the dimensions of devices are consistently scaled down proportionally. However, this proportional scaling is not ideal, as not all parameters reduce proportionally. The lateral electric field (E_x) strength in the channel of a device increases as the dimensions are scaled down, with the strongest field occurring near the drain. When the characteristic dimensions of a device are reduced to a certain extent, a high electric field is generated between the source and drain, leading to carriers being accelerated into hot carriers (HCs) as they move. When these HCs have enough energy to overcome the Si-SiO_2 barrier height (3.5 eV), they can directly inject or tunnel into SiO_2, causing damage to the gate oxide and leading to device performance degradation or damage. This phenomenon is known as the HC effect.

The LDD structure utilizes two different doping concentrations in the source and drain regions. The doping concentration is lower near the channel and higher near the source and drain electrodes. This creates a gradient in doping concentration between the source/drain region and the channel, acting as a buffer for the source/drain electric field. It can reduce the peak electric field at the source and drain electrodes, decrease the generation and injection of hot electrons, and thereby enhance the stability of the device [1].

8.2.1. Fabrication Process of Lightly Doped Drain Structure Thin-Film Transistors

Initially, a 100 nm layer of SiO_2 is deposited on a glass substrate using plasma-enhanced chemical vapor deposition (PECVD) as a buffer layer. Subsequently, a 50 nm thick amorphous silicon (a-Si) film is deposited at 380°C using PECVD. The a-Si film is then subjected to dehydrogenation annealing at 450°C in a furnace. The a-Si is patterned through a sequence of processes, including spin-coating photoresist, pre-baking, exposure, development, etching, and cleaning. The a-Si film is then crystallized using a 308 nm XeCl excimer laser with a linear beam power of 350 mJ/cm². Another 100 nm thick SiO_2 layer is deposited via PECVD to serve as the gate insulator (GI).

A 300 nm thick layer of molybdenum is then deposited using magnetron sputtering and patterned as the gate electrode through photolithography and etching. Phosphorus ions are implanted using a mass-separated ion implanter to form n-

regions in the LDD areas and n^+ regions at the source and drain, followed by a furnace anneal to activate the dopants. The final LDD structure TFT is shown in Fig. (**8.1**).

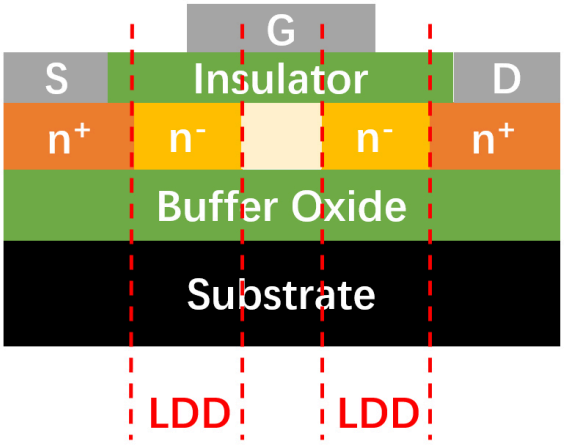

Fig. (8.1). LDD structure in TFT.

8.2.2. Effect of Lightly Doped Drain Structure on Thin-Film Transistor Reliability

When discussing the reliability of TFTs, two key parameters of the LDD structure play a crucial role: the length of the LDD and the doping concentration. These parameters significantly affect the electrical performance and reliability of TFTs.

The LDD structure introduces a lightly doped region that moderately increases resistance, leading to a more uniform electric field distribution near the drain and preventing the occurrence of high electric fields. The transfer curve of a TFT without an LDD structure is shown in Fig. (**8.2a**), where the curve tails up due to the high electric field at the drain, resulting in a pronounced drain-induced barrier lowering (DIBL) effect and a higher off-state current (I_{off}). The transfer characteristic curve of a TFT with an LDD structure is shown in Fig. (**8.2b**). The presence of the lightly doped source and drain regions disperses the electric field, making the distribution more uniform and reducing the electric field at the drain. Consequently, the I_{off} of the LDD structure TFT is lower. The transfer curves exhibit consistent behavior across V_{ds} of 0.1 V, 5 V, and 10 V [2]. Similarly, by incorporating the LDD structure, the shift in threshold voltage (V_{th}) can be reduced, but this also results in lower mobility and on-state current (I_{on}) [3].

CHAPTER 9

Summary

9.1. SUMMARY OF RELIABILITY OF THIN-FILM TRANSISTORS

This book primarily uses silicon-based (Si-based) thin-film transistors (TFTs) and metal oxide (MO) TFTs as examples to thoroughly explain the materials, structures, and working principles of TFT devices. It also provides a detailed discussion of the degradation phenomena, mechanisms, and improvement methods for TFT reliability across different types.

The book begins with an introductory chapter on the history of TFT development, followed by a brief overview of TFT classification and applications. It then delves into several common TFT structures, detailing the typical structures of Si-TFTs and MO-TFTs, as well as their fabrication methods. The book proceeds to discuss various common applications of TFTs, with an emphasis on the impact of reliability in these applications.

Subsequently, Chapter 2 focuses on reliability issues in TFTs, starting with the characterization of basic TFT performance, emphasizing measurement and analysis methods for transfer and output characteristic curves. It then highlights typical defects found within Si-TFTs and MO-TFTs, concluding with a summary of several typical degradation mechanisms in TFTs. Chapter 2 serves as the theoretical foundation for the entire book.

After an overall introduction to TFT reliability, Chapter 3 explores various methods for analyzing TFT reliability. It covers the characterization of basic transfer characteristics, including analysis methods for the on-state and subthreshold swing (*SS*) of the transfer curve before and after degradation. The chapter also introduces the analysis method for TFT's capacitance-voltage (CV) characteristics and highlights several methods for extracting defect density from CV curves. Additionally, it discusses low-frequency noise analysis methods and key application formulas, followed by an introduction to various TFT thin-film characterization techniques, including x-ray photoelectron spectroscopy, transmission electron microscopy, x-ray diffraction, scanning electron microscopy, atomic force microscopy, and Raman analysis. The chapter concludes with two simulation methods: semiconductor device simulation and thermal simulation.

Chapter 4 focuses on the degradation conditions and mechanisms of TFTs under direct current (DC) stress, detailing the typical degradation scenarios and special cases for Si-TFTs and MO-TFTs under gate bias stress, hot carrier (HC) stress, and self-heating (SH) stress.

Chapters 5 and 6 provide an in-depth look at the degradation of TFTs under different alternating current (AC) stress conditions. They begin with a brief overview of TFT degradation under typical single-ended pulse stress and analyze how changes in pulse parameters affect device degradation. A non-equilibrium PN junction AC reliability model is introduced to explain AC degradation under various conditions. Since TFTs often operate in more complex pulse environments, Chapter 7 discusses TFT degradation under DC bias AC stress, dual-end AC stress, and ultrafast AC stress, presenting an enhanced non-equilibrium PN junction AC reliability model.

Chapter 7 primarily examines the impact of different environmental factors on TFT reliability, discussing the effects of temperature, light exposure, and humidity on device reliability. Chapter 8 introduces several methods for improving TFT reliability, focusing on structural modifications, including the LDD and BG structures, as well as other improvement methods.

Overall, this book provides a comprehensive introduction to the degradation phenomena and principles of TFT reliability, supplemented by an overview of necessary foundational knowledge. The content presented serves as a theoretical basis for research and production work related to TFT reliability studies.

9.2. FUTURE WORK ON THE RELIABILITY OF THIN-FILM TRANSISTORS

This book primarily focuses on the reliability analysis of mainstream Si-based TFT (Si-TFT) devices and MO TFT (MO-TFT) devices. As a new generation of TFTs, MO-TFTs offer advantages such as low-temperature fabrication and extremely low leakage current that are difficult for polycrystalline silicon (poly-Si) TFTs to achieve. However, reliability research for MO-TFTs is still not comprehensive. In the case of DC gate bias stress, the same stress voltage leads to both positive and negative shifts in different types of MO-TFTs. Although numerous mechanisms have been proposed to explain these phenomena, there is still a lack of a unified model to predict when MO-TFTs will exhibit negative or positive shifts under gate bias stress.

Similarly, the reliability of MO-TFTs is a major obstacle to their practical application. For basic gate bias stress, poly-Si TFTs typically require high gate voltages or high-temperature treatment to cause significant device degradation, while MO-TFTs often show noticeable degradation at gate voltages above 20 V. Additionally, due to the conduction mechanisms of MO-TFTs, those with higher mobility often suffer from poorer reliability. This is why, despite the availability of high-mobility MO-TFTs, IGZO TFTs still dominate commercial applications. Improving the reliability of MO-TFTs is one of the key research areas for future MO-TFT development.

It is also worth noting that most current reliability analyses are qualitative, which can guide the improvement of TFT device reliability in commercial applications to some extent. However, to further expand on these reliability analyses, such as predicting the working life of TFTs or the overall display, or to compensate for TFT degradation specifically, quantitative research on device degradation is required. This includes the study of analytical models for device performance and the development of degradation analysis models. While there is a substantial amount of work on the initial analytical models for TFTs, which can well fit the performance changes of devices in on-state, off-state, and subthreshold state, research on analytical models for degraded devices is relatively scarce, with most focusing on DC studies. There is almost no research on analytical models for AC reliability

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