NANO-FET DEVICES: MINIATURIZATION, SIMULATION, AND APPLICATIONS - PART 1

Editors:
Dharmendra Singh Yadav
Prabhat Singh

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Nano-FET Devices: Miniaturization, Simulation, and Applications

(Part 1)

Edited by

Dharmendra Singh Yadav

Department of Electronics and Communication Engineering,
National Institute of Technology,
Kurukshetra, Haryana 136119,
India

&

Prabhat Singh

Department of Electronics and Communication Engineering,
B.R. Ambedkar National Institute of Technology,
Jalandhar, Punjab,
India

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Editors: Dharmendra Singh Yadav & Dharmendra Singh Yadav

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FOREWORD

Welcome to the world of Nano-FET Devices, where innovation meets miniaturization at the nanoscale frontier. The history of Nano Field-Effect Transistor (FET) devices is characterized by a progression from traditional FETs to the exploration of nanoscale materials and quantum effects. Beginning with the development of Metal-Oxide-Semiconductor FETs (MOSFETs) in the 1950s, the quest for miniaturization led to the investigation of Single Electron Transistors (SETs), semiconductor Quantum Dots (QDs), Carbon Nanotubes (CNTs), Nanowires, and Graphene FETs (GFETs) over subsequent decades. These advancements, driven by the desire for higher performance and energy efficiency, have laid the groundwork for Beyond CMOS technologies, pushing the boundaries of device miniaturization and functionality towards new frontiers in electronic engineering. Not just limited to engineering and material based study, the innovations in Nano-FET have allowed us to come up with a logical deduction towards understanding the complex and multiple associations within the biomolecules and biological applications.

As technology advances, the demand for smaller, faster, and more efficient electronic devices grows incessantly. Nano-FETs represent a paradigm shift in this quest for miniaturization, offering unprecedented control, performance, and versatility in electronic components. From ultra-high-speed computing to ultra-low-power sensors, Nano-FETs are at the forefront of innovation, driving the evolution of electronic devices and systems. This book embarks on a journey into the fascinating realm of FETs at the nano-level, diving deep into their principles, possibilities, and profound impact on modern electronics.

Simulation plays a pivotal role in modern device design, and this book equips readers with the tools and methodologies to simulate nano FETs accurately. From quantum mechanical simulations to advanced device modeling, readers gain a deep understanding of how nano FETs behave under different operating conditions, enabling precise performance predictions and optimizations. The applications section bridges theory with real-world implementations, showcasing how nano FET devices are revolutionizing diverse fields such as integrated circuits, sensors, biomedical devices, and more. Case studies and examples elucidate the impact of nano FETs on cutting-edge technologies, inspiring readers to explore new possibilities and innovations.

Whether you're a seasoned researcher, an aspiring engineer, or simply curious about the future of electronics, this book invites you to explore the captivating world of Nano-FET Devices. This book unravels the mysteries, unlock the potentials, and embark on a journey of discovery at the frontier of miniaturization and innovation.

Naveen Kumar
Department of Electronics and Nanoscale Engineering,
University of Glasgow,
Glasgow, G128QQ,
United Kingdom

PREFACE

Millions of transistors comprise an integrated circuit. Transistors are the essential aspects of all modern electrical components and electronic devices. Transistor size has been progressively shrunk as the VLSI industry grows to integrate more functionality onto a silicon wafer and minimize circuit power consumption. Nano-FET devices are being realized using various materials with different structures, with promising results. Novel nano-FET devices should be an excellent candidate to replace the existing technologies for low-power and high-frequency applications with reduced time delay in circuit applications.

The relentless pursuit of miniaturization in semiconductor technology has led to the emergence of nano FETs as pivotal components in modern electronic systems. This book aims to provide a comprehensive overview of nano FET devices, from their theoretical foundations to application implementations. Due to the enormous study of Nano-CMOS and post-CMOS technologies and the lack of a comprehensive guidebook, research articles are now the cornerstone for the knowledge of novel design based on the fundamentals of Nano-FET devices. As a result, this book outlining the essential characteristics of Nano-CMOS and post-CMOS technologies will benefit engineers who must understand the fundamentals and scholars developing/implementing Nano-CMOS and post-CMOS devices and its applications. This book, Nano-FET Devices: - Miniaturization, Simulation, and Applications, is intended to fulfil this requirement for the device research community.

In the opening chapters, readers will embark on a journey through the basic concepts of FETs, understanding how these devices operate and their significance in electronic engineering. Building upon this foundation, the book delves into the unique characteristics of nano FETs, including quantum effects, scaling considerations, and material properties that define their behavior at the nanoscale.

This book is a concise benchmark for beginners who are just getting started with Nano-FET Devices and its application with recent advancement and those who want to design integrated circuits using novel FET devices. We hope that "Nano-FET Devices: Miniaturization, Simulation, and Applications" serves as a valuable resource for researchers, engineers, and students interested in unlocking the potentials of nano FET technology. May this book inspire new discoveries, innovations, and advancements at the forefront of electronic engineering.

Dharmendra Singh Yadav
Department of Electronics and Communication Engineering
National Institute of Technology
Kurukshetra, Haryana 136119
India

&

Prabhat Singh
Department of Electronics and Communication Engineering
B.R. Ambedkar National Institute of Technology
Jalandhar, Punjab
India

DEDICATION

I would like to dedicate and express my hearty gratitude towards my respected parents, Uncle, aunty, younger brothers, sisters for their affection and persistent efforts in my education. Also dedicated to my wife and our loving son Armaan Singh for their everlasting supports, encouragements and understanding. This work is dedicated to my family and others who have always been as source of my continued efforts for academic excellence. Over to all infinite gratitude flows to the almighty for the countless blessings bestowed upon us.

— Dharmendra Singh Yadav

I dedicate this book to my loving mother, Shakuntala Singh, father Dinesh Singh, wife Sadhana Singh and brother Prasoon Singh, as a token of my appreciation for everything you have done and continue to do for me. Your love and support are the foundation of my success, and I am blessed to have you as a part of my life. I would like to thank Dr. Ashish Raman and Dr. Navjeet Bagga for their unconditional guidance. Your love and belief in me mean everything. This book is dedicated to you as a symbol of my gratitude for all you've done.

— Prabhat Singh

List of Contributors

Agnibha Dasgupta	GE Vernova, DIG Grid Support, Bengaluru, Karnataka, India
Ashish Kumar Singh	Department of Electronics and Communication Engineering, Chitkara University Institute of Engineering and Technology, Chitkara University, Punjab, India
Abhinav Rajyan	Department of Electronics and Communication Engineering, School of VLSI Design and Embedded Systesm, NIT Kurukshetra, Haryana, India
Brinda Bhowmick	Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam 788010, India
B. Karthikeyan	Department of ECE, Velammal College of Engineering and Technology, Madurai, Tamil Nadu, India
Chandani Dubey	Department of Electrical Engineering, Indian Institute of Technology, Delhi, India
C. Muthu Pandian	Department of ECE, Velammal College of Engineering and Technology, Madurai, Tamil Nadu, India
Dilip Singh	Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur, India
Girdhar Gopal	School of Electronics, IIIT Una, Himachal Pradesh 177209, India
Gaurav Saini	Department of Electronics and Communication Engineering, School of VLSI Design and Embedded Systesm, NIT Kurukshetra, Haryana, India Department of ECE, NIT Kurukshetra, Haryana, India
Gargi Khanna	Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur, India
G. Annam	Department of ECE, Velammal College of Engineering and Technology, Madurai, Tamil Nadu, India
Karthik Nasani	Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam 788010, India
K.M.D Sridharshan	Department of ECE, Velammal College of Engineering and Technology, Madurai, Tamil Nadu, India
Prabhat Singh	Department of Electronics and Communication Engineering, B.R Ambedkar National Institute of Technology, Jalandhar, Punjab, India
Priya Kaushal	Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur, India
Puspa Devi Pukhrambam	Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam 788010, India
P. Suveetha Dhanaselvam	Department of ECE, Velammal College of Engineering and Technology, Madurai, Tamil Nadu, India
Ramesh Kumar	Department of Electronics and Communication Engineering, Chitkara University Institute of Engineering and Technology, Chitkara University, Punjab, India Department of Electronics Engineering, IIT (BHU), Varanasi, UP, India

Soumya Sen Department of Computer Science & Engineering, University of Engineering and Management, Jaipur, Rajasthan, India

Shruthi Gajula Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam 788010, India

Shivalika Sinha Department of Electronics Engineering, IIT (BHU), Varanasi, UP, India

Satyabrata Jit Department of Electronics and Communication Engineering, Chitkara University Institute of Engineering and Technology, Chitkara University, Punjab, India

Sunil Dhawan Department of Electronics and Communication Engineering, Chitkara University Institute of Engineering and Technology, Chitkara University, Punjab, India

S. Subashi Department of ECE, Velammal College of Engineering and Technology, Madurai, Tamil Nadu, India

Tarun Varma Department of Electronics and Communication Engineering, Malaviya National Institute of Technology Jaipur, Rajasthan 302017, India

Vikas Malhotra Department of Electronics and Communication Engineering, Chitkara University Institute of Engineering and Technology, Chitkara University, Punjab, India

Vasunthra R.S. Department of ECE, Velammal College of Engineering and Technology, Madurai, Tamil Nadu, India

CHAPTER 1

Nanoelectronic Horizons: Exploring the Future of FET Technologies with Nanostructures

Soumya Sen[1,*], Agnibha Dasgupta[2], Prabhat Singh[3] and **Ashish Raman[3]**

[1] *Department of Computer Science & Engineering, University of Engineering and Management, Jaipur, Rajasthan, India*

[2] *GE Vernova, DIG Grid Support, Bengaluru, Karnataka, India*

[3] *Department of Electronics and Communication Engineering, B.R Ambedkar National Institute of Technology, Jalandhar, Punjab, India*

Abstract: The chapter "Nanoelectronic Horizons" presents a forward-looking exploration of the symbiotic relationship between Field-Effect Transistor (FET) technologies and nanostructures, offering a glimpse into the future of nanoelectronics. Acknowledging the foundational role of FETs in modern electronics, this chapter unfolds the transformative potential that emerges with the integration of nanostructures.

Beginning with a historical overview, the narrative traces the evolution of FET technologies, setting the stage for the contemporary landscape. The foundations of Field-Effect Transistors, including their diverse types and applications, are succinctly explained. The subsequent transition into the realm of nanostructures unveils their unique properties at the nanoscale and establishes them as enablers of advanced functionalities in electronics. The chapter delves into the synergies between FET technologies and nanostructures, emphasizing their role in pushing the boundaries of traditional electronic capabilities. Exploration of recent advancements reveals cutting-edge developments in nanostructure integration, showcasing real-world applications and breakthroughs in research. Challenges and potential solutions in merging these technologies are examined, paving the way for a deeper understanding of the intricate landscape. As the narrative unfolds, readers are guided through the potential impact on various industries, the environmental considerations, and the regulatory landscape. The chapter concludes by envisioning the future prospects of FET technologies linked to nanostructures, offering insights into market trends, technological growth areas, and the societal implications of this transformative journey. Lastly, this chapter serves as a compass guiding readers through the evolving landscape of FET technologies with nanostructures, beckoning towards a future where innovation and collaboration redefine the horizons of nanoelectronics.

***Corresponding author Soumya Sen:** Departmnent of Computer Science & Engineering, University of Engineering and Management, Jaipur, Rajasthan, India Tel: +91-9830980381; E-mail: sensoumya8730@gmail.com

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Keywords: Electronics, FET technologies, Nanoelectronics, Nanostructures, Nanoscale.

INTRODUCTION

The integration of Field-Effect Transistor (FET) technologies with nanostructures represents a captivating frontier in the realm of electronics, offering unprecedented opportunities for innovation and transformative advancements. This book chapter embarks on a comprehensive exploration of the dynamic intersection between FET technologies and nanostructures. Through a focused lens, we aim to unravel the synergies, challenges, and possibilities that arise when these two cutting-edge domains converge, presenting readers with a nuanced understanding of the current state and future directions in nanoelectronics.

At the heart of this chapter lies a dedicated inquiry into the confluence of both. We will delve into the intricacies of this interdisciplinary fusion, examining how the combination of advanced transistor technologies with nano-scale materials and architectures can redefine the landscape of electronic devices. The chapter aims to illuminate the key principles, methodologies, and emerging trends that drive this convergence, providing readers with insights into the potential applications and implications for the future of electronics.

To appreciate the significance of the present-day integration of FET technologies with nanostructures, a brief historical overview is imperative. The narrative begins with the early developments of Field-Effect Transistors, tracing their evolution from the pioneering work of scientists like Lilienfeld and Bardeen-Brattain. The journey through time encompasses pivotal milestones such as the advent of MOSFETs and the subsequent dominance of CMOS technology, laying the foundation for the intricate electronic systems prevalent today.

Simultaneously, we explore the rise of nanostructures, witnessing the shift towards materials and architectures at the nanoscale. From the initial investigations into quantum dots to the versatility offered by nanowires and the emergence of two-dimensional materials, the historical narrative converges with the contemporary drive towards miniaturization and enhanced functionality. This historical context sets the stage for the present-day convergence of FET technologies and nanostructures, highlighting the cumulative efforts and discoveries that have shaped the trajectory of modern-day technology.

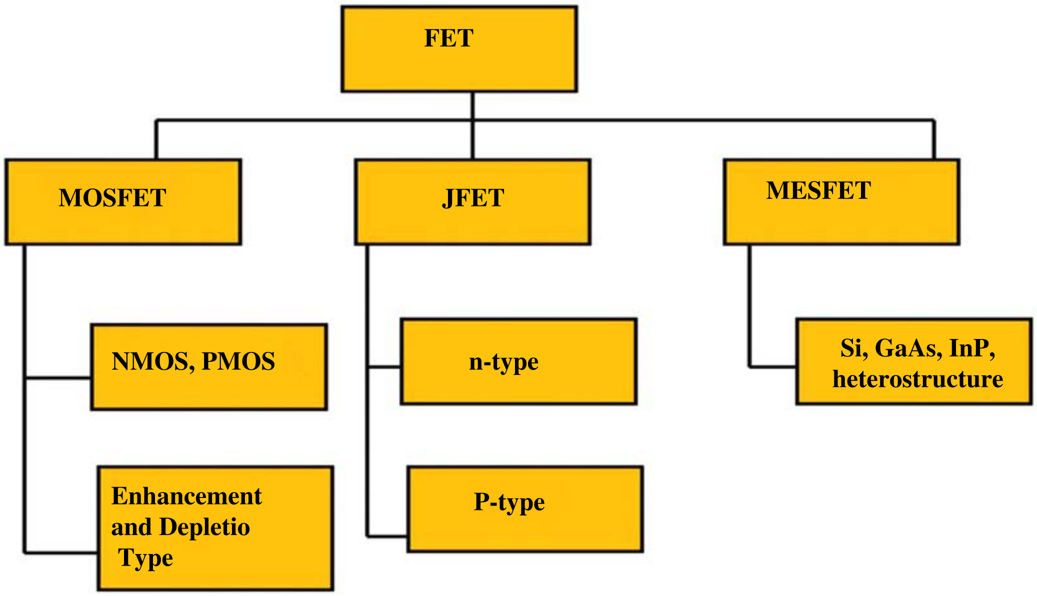

Fig. (1). Modern-day FET Technologies.

As we navigate through the pages of this chapter, the synthesis of historical insights with contemporary developments will illuminate the transformative potential embedded within the intersection of FET technologies rendered in Fig. (**1**) and nanoscale devices. From fundamental principles to cutting-edge applications, the exploration aims to provide readers with a holistic understanding of the dynamic interplay between these two realms, inspiring further inquiry and innovation in the field of nanoscience [1-4, 5-8].

FOUNDATIONS OF FET TECHNOLOGIES

The historical development of Field-Effect Transistor (FET) technologies unfolds as a captivating narrative that has played a pivotal role in shaping the landscape of modern electronics. Rooted in the theoretical musings of Julius Lilienfeld in the early 20th century, the concept of a field-effect device began to take form. However, it was not until the post-World War II era that tangible progress was made. The groundbreaking moment came with the advent of the point-contact transistor by John Bardeen and Walter Brattain in 1947. This initial foray into transistor technology laid the groundwork for further exploration and innovation [9-18].

CHAPTER 2

From CMOS to TFET: Technological Scalability and Performance Concerns Pertaining to Moore's Law

Girdhar Gopal[1,*] and **Tarun Varma**[2]

[1] *School of Electronics, IIIT Una, Himachal Pradesh 177209, India*

[2] *Department of Electronics and Communication Engineering, Malaviya National Institute of Technology Jaipur, Rajasthan 302017, India*

Abstract: Moore's law has contributed to a significant factor behind the ongoing shrinking of transistors in CMOS technology since its inception in the 1960s. Dennard *et al*.'s scaling theory from 1974 illustrates how cost, performance, and power can be enhanced in solid-state devices while maintaining fundamental MOSFET operating characteristics. In the past, the regulation of dynamic power was governed by Moore's law. However, as leakage increases with decreasing geometries, quiescent power consumption becomes the predominant factor in microprocessor design. Short channel issues like DIBL, SS, and hot electron effect may all have a detrimental influence on MOS device performance. Because of these effects, CMOS technology has hurdles, and TFETs may overcome SS limits, making them a promising option for low-power standby uses. Finally, we discuss the possibilities beyond CMOS technology, detailing the difficulties and prospects for technological advancement. This chapter gives a brief summary of current developments in device development with an emphasis on Tunnel FETs for upcoming circuits.

Keywords: CMOS, MOSFET, TFET, Transistors.

BRIEF OVERVIEW

Nanoelectronics is the combination of nanotechnology with electronics. Electronics involves the manipulation of electron flow in various environments, such as vacuum, inert gas, or solid-state semiconductors, to create devices like diodes and transistors. It also includes building and arranging circuits with these parts to carry out particular functions in power conditioning, computation, communication, and information processing. Nanoelectronics is driving the process of making gadgets

*** Corresponding author Girdhar Gopal:** School of Electronics, IIIT Una, Himachal Pradesh 177209, India; E-mail: 2019rec9550@mnit.ac.in

smaller to the point where they reach their fundamental physical limits. Moore's law, a well-known principle, predicts that the number of transistors per square inch in an integrated circuit would double annually. There are three well-defined sub-domains of nanoelectronics. These categories are known as [1]: Beyond CMOS, More-than-Moore, and More Moore. "More Moore" refers to the increasing packing density of devices that follow Moore's law. Moreover, the More Moore Sub-domain refers to the element quantities that are approaching giga-scale magnitudes when circuits with nanoscale parts are built. To lower the cost per unit of capability, advanced CMOS technology will be greatly improved. This will affect 70 percent of the market, which comprises memory, microprocessor chips, and digital logic circuits. The pathway towards achieving immense complexity is referred to as the "More Moore" approach [2].

When additional features are included that defy Moore's law's scaling principles—such as sensors, RF, and power conditioning circuits—the phrase "More than Moore" is used. The term "more-than-Moore" is an idea in the electronics profession that goes beyond simple scaling to incorporate extra features and functionalities into semiconductor devices. The integration of mechanical, biological, and electronic circuits with analog/RF circuits is referred to as a sub-domain. The two interconnected strategies for Moore scaling beyond CMOS technology are depicted in Fig. (**1**).

Under the "Beyond CMOS" category are developing devices such as single-electron transistors and molecular electronic devices. These devices are expected to reach higher integration levels than CMOS technology. Electronics that take advantage of developing state variables, like spin, molecular state, photons, and many other comparable elements, fall under this sub-domain. Molecular electronics and spintronics are two examples. Thus, the area of nanoelectronics will witness the introduction of completely new nanoscale devices through the "beyond CMOS" sub-domain.

An important objective of "Beyond CMOS" is to develop scalable volatile and non-volatile memory technologies that may effectively replace SRAM and NAND flash memory in suitable usages. The fundamental elements of these new memories consist of innovative memory devices and selection devices. Another significant obstacle is to expand the use of CMOS technology, which is already very scalable, into new areas of application. The next logic and information processing devices will consist of expanded CMOS devices and/or devices that go beyond CMOS technology.

CMOS technology has significantly contributed to reducing the size of electronic devices, enabling the development of small but powerful digital/analog circuits. CMOS ICs are scaled down in size to enhance their switching speed, functionality, and packaging density [3]. Punch-through, substrate bias amplification, threshold voltage roll-off, drain-induced barrier lowering (DIBL), and other phenomena are caused by short channel effects (SCEs) due to the the close distance of the source and drain [4-5]. Because it is difficult to limit the fast rise in the OFF-state leakage current and lower integrated circuit supply voltage to 0.5 V, the device's performance deteriorates as power consumption rises [6-7]. Therefore, cutting down on power consumption is a major goal of contemporary low-power technologies. As per the ITRS report, semiconductor devices should be able to achieve gate lengths of 20 nm or less in the near future.

ITRS has predicted that Tunnel Field Effect Transistors (TFETs) are the best suitable option for subthreshold slopes below 60mV/decade at room temperature.

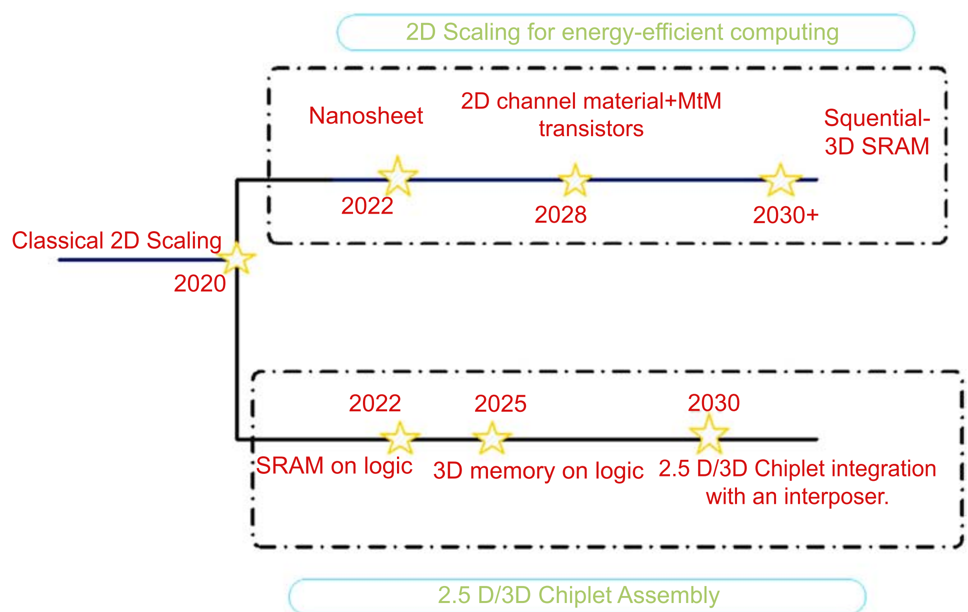

Fig. (1). Two complementary routes for more Moore scaling.

Scaling Trends and Challenges

The goal of this section is to present engineers with another option for designing devices that can meet the high requirement for modern rechargeable portables by resolving most of the scaling challenges and increasing productivity in a small, low-

CHAPTER 3

Metasurface-Based Realization of Photonic Crystal: Design, Fabrication, and Applications

Chandani Dubey[1,*], **Priya Kaushal**[2], **Dilip Singh**[2] and **Prabhat Singh**[3]

[1] *Department of Electrical Engineering, Indian Institute of Technology, Delhi, India*

[2] *Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur, India*

[3] *Department of Electronics and Communication Engineering, B.R. Ambedkar National Institute of Technology, Jalandhar, Punjab, India*

Abstract: The present study investigates the use of metasurfaces in the fabrication of photonic crystals to harness their unique features for improved optical functions. Metasurfaces, comprised of subwavelength nanostructures, offer unprecedented control of polarization, amplitude, and phase. When combined with the inherent characteristics of photonic crystals, such as bandgap formation and light confinement, novel opportunities arise for manipulating and guiding light at the nanoscale. The present work investigates the design principles, fabrication techniques, and potential applications of metasurface-enhanced photonic crystals. This chapter highlights the hybrid integration of metasurface techniques with photonic crystals and covers essential design issues. It highlights nonlinear optical phenomena, increased light-matter interactions, and tuneable bandgaps in metasurface-enhanced photonic crystals. This paper investigates the reflection and transmission characteristics of metasurface-enhanced photonic crystals, shedding light on their unique optical properties and potential applications. Furthermore, the research investigates many applications, such as sensors, light emission devices, and information processing, highlighting the transformational potential of this combined method. Through theoretical modeling and experimental validation, we present a comprehensive analysis of how metasurface enhancements influence the reflection and transmission spectra, including the emergence of tuneable bandgaps and tailored optical responses. This chapter advances the understanding of metasurface-based photonic crystals by providing a roadmap for academics and engineers in the fast-expanding field of nanophotonics through a critical assessment of problems and future objectives. By providing insights into the intricate interplay between metasurfaces and photonic crystals, this work contributes to the advancement of nanophotonics and lays the foundation for the development of novel devices with enhanced optical functionalities.

Keywords: Metamaterials, Metasurface, Photonic time crystal, Transfer matrix.

*** Corresponding author Chandani Dubey:** Department of Electrical Engineering, Indian Institute of Technology, Delhi, India; E-mail: Chandanidubey13@gmail.com

Dharmendra Singh Yadav & Prabhat Singh (Eds.)

INTRODUCTION

In the fields of photonics and optical engineering, metasurfaces and photonic crystals are both innovative concepts that provide special powers for directing and modifying light. Metasurfaces are two-dimensional arrays of structures at subwavelength scales that can manipulate electromagnetic wave characteristics [1]. Periodic structures known as photonic crystals display photonic band gaps, which are frequencies at which the propagation of electromagnetic waves, including light, is prohibited. Photonic crystals, such as electronic band gaps in semiconductors, can have band gaps for specific wavelengths of light. Their ability to precisely control light flow makes it possible to create optical devices with special qualities [2]. With the use of photonic crystals, waveguides that direct light through a crystal without experiencing propagation losses can be made [3-4]. They enable it to be possible to build optical cavities that can house lasers and other light-emitting equipment. As filters, photonic crystals can let some wavelengths through while inhibiting others. At the subwavelength scale, metasurfaces allow control of the amplitude, phase, and polarization of light [5-7]. They are typically flat and thin, allowing them to be integrated into a variety of devices. Metasurfaces can be used to make ultrathin lenses with exceptional focusing characteristics [8-10]. They allow for exact control of light polarization. Holography uses metasurfaces to manipulate light and generate 3D images. Researchers have investigated the possibility of combining the benefits of metasurfaces and photonic crystals to produce more adaptable and efficient devices [11-14]. Band gaps in photonic crystals can be dynamically adjusted by integrating metasurfaces with customizable characteristics. Metasurfaces offer small and flat solutions that can aid in the miniaturization of photonic crystal devices. Photonic crystals can have their response tailored to particular wavelengths and applications thanks to metasurfaces. Multifunctional photonic crystal devices that are capable of beam steering, polarization control, and focusing can be created by integrating metasurfaces [15-17].

Photonic time crystals (PhTC) are synthetic substances with EM characteristics that are homogeneous in space while variable in time. The production of these particular materials, as well as the experimental observation of material physics, is extremely difficult [18-19]. We expand the perception of PhTC to metasurfaces in this book chapter. We observe that time-varying metasurfaces retain important physical aspects of volumetric time crystals, such as the generation of momentum bandgaps for surface waves as well as for free-space waves. The momentum bandgap is easily accessible through free-space excitations, leading to a simplified implementation and utilization of the crystal [20-22]. Our achievement marks the initial demonstration of exponential wave amplification occurring within a momentum bandgap, achieved through the design of a microwave metasurface. Fig. (**1**) represents the schematic diagram of metasurface-based photonic crystal.

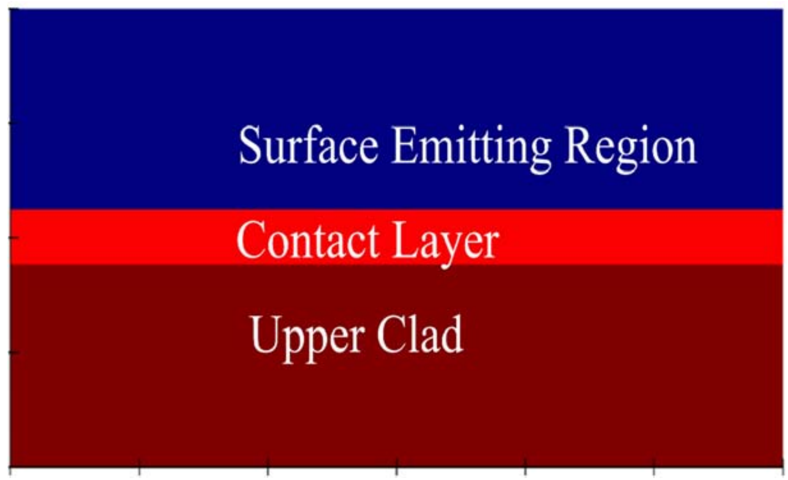

Fig. (1). Schematic representation of Metasurface-Based Photonic Crystal.

Time crystals require a rapid temporal change in material properties at about twice the operating frequency (f) of the probing EM field. However, due to the finite excitation and recombination periods in these materials (now around a few terahertz), generating such rapid oscillations is a challenging task [23-26]. Photonic crystals are substances that display a repetitive fluctuation in their dielectric constant at a scale similar to the wavelength of light [27-29]. The periodic structure creates a bandgap for certain frequencies of electromagnetic waves, much like the electronic band gap in semiconductors. Photonic crystals have control over the flow of light, leading to various optical phenomena and applications. Photonic crystals feature a periodic arrangement of dielectric materials, and the refractive index fluctuates in space with a specific periodicity [30-31]. The periodic structure is often lattice-based, akin to crystal formations in solid-state physics. The key defining characteristic of photonic crystals is the existence of a photonic bandgap, which illustrates the frequency range where the propagation of light is inhibited. Photonic band gaps are similar to electronic band gaps in semiconductors, but they exist in the optical frequency spectrum [32-35]. A defining feature of photonic crystals is their possession of a photonic bandgap, which represents a frequency range where light propagation is effectively blocked. Photonic bandgaps are identical to electronic bandgaps in semiconductors, but they exist in the optical

CHAPTER 4

Unravelling Reliability Challenges and Scalability Effects in HJ-DGV-TFET: A Study of Hetero Buried and Stacked Buried Configurations

Karthik Nasani[1,*], **Brinda Bhowmick**[1], **Puspa Devi Pukhrambam**[1] and **Shruthi Gajula**[1]

[1] *Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam 788010, India*

Abstract: This research aims to explore the complex challenges regarding reliability and scalability in Heterojunction Dual Gate Vertical Tunnel Field Effect Transistors (HJ-DGV-TFET). Specifically, it focuses on comparing the hetero buried and stacked buried configurations. The study thoroughly examines factors affecting reliability, such as traps, noise susceptibility, lateral straggle, self-heating, and scalability effects. These factors collectively impact the performance and lifespan of advanced electronic devices. Through extensive simulations under different operational conditions, this investigation quantifies and compares the influence of these reliability issues in both configurations. Additionally, the study delves into how HJ-DGV-TFETs maintain their reliability as technology continues to scale down.

Keywords: Hetero buried oxide, HJ-DGV-TFET, Noise, Oxide thickness, Stacked buried oxide, Source doping, Traps, Temperature variations.

INTRODUCTION

Improved performance, lower power consumption, and increased reliability have been the unwavering goals driving the development of semiconductor devices. TFETs have attracted a lot of attention in this technological quest because they can overcome the drawbacks of old MOSFETs [1-6]. With its unique design that makes use of heterostructures to improve device characteristics, the HJ-DGV-TFET has become a highly interesting avenue for innovation in the field of TFETs [7-9].

The Hetero Buried Oxide HJ-DGV-TFET and the Stacked Buried Oxide HJ-DGV-TFET are two particular configurations within the HJ-DGV-TFET domain that will

* **Corresponding author Karthik Nasani:** Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, Assam 788010, India; E-mail: karthik21_rs@ece.nits.ac.in

be thoroughly explored and compared in this chapter. These combinations are examples of sophisticated design techniques that improve TFET performance benchmarks by utilizing the special qualities of buried oxide layers and heterojunctions. The nuances of these arrangements will be dissected in the following sections, along with their possible uses, advantages, and implications for the advancement of semiconductor technology [10].

With its heterojunction architecture, the Hetero Buried Oxide HJ-DGV-TFET expands the range of TFETs by utilizing a variety of semiconductor materials to take advantage of different bandgaps. The addition of a heterostructure improves the properties of charge transport and allows for more accurate control over the tunneling process. The buried oxide layer is a key component in this arrangement, as it is positioned to adjust the height of the tunneling barrier. This modulation not only improves subthreshold swing but also raises the device's overall efficiency [11].

The Stacked Buried Oxide HJ-DGV-TFET, on the other hand, takes a novel approach by stacking several oxide layers. The goal of this design approach is to optimize the device's electrostatics and tunneling properties. Engineers can control the tunneling barrier further by stacking oxide layers, which allows for a more subtle balance between subthreshold swing and ON state current. This stacked arrangement offers a viable path for performance metric optimization by resolving enduring issues with conventional TFET designs [12, 13].

Our goal is to examine every configuration in detail and analyze how it affects important performance metrics like ON state current, ON-OFF current ratio, and subthreshold swing as we begin this comparative investigation. We will also assess their suitability for incorporation into modern electronic systems, taking into account aspects like their scalability, manufacturability, and flexibility to accommodate a range of application scenarios.

The objective of this comparative analysis is to make a significant contribution to our collective understanding of advanced TFET designs. Through our analysis of the Hetero Buried Oxide and Stacked Buried Oxide HJ-DGV-TFET topologies, we hope to shed light on their individual benefits, possible drawbacks, and impacts on the semiconductor industry as a whole. By taking this journey, we hope to strengthen the groundwork for upcoming advancements in semiconductor technology and bring in a new era of sophisticated and effective electronic devices [14, 15].

This study compares two different configurations, the hetero-buried and stacked buried setups, in order to provide a thorough analysis of the issues related to the scalability and reliability of HJ-DGV-TFETs. The aforementioned configurations embody sophisticated design paradigms, each offering distinct benefits and difficulties in terms of maximizing transistor performance. Factors like self-heating, lateral straggle, noise susceptibility, traps, and scalability effects affect an electronic device's reliability and provide insight into the complex dynamics of HJ-DGV-TFET reliability. This work thoroughly investigates these variables in both the hetero-buried and stacked buried configurations. The inquiry also tackles the issue of how HJ-DGV-TFETs continue to be reliable in spite of constant reductions in semiconductor technology. As the industry moves towards smaller scales and higher integration densities, it becomes increasingly important to comprehend the resilience and adaptability of HJ-DGV-TFETs. By means of comprehensive simulations carried out in various operational scenarios, this investigation attempts to clarify the complexities surrounding reliability issues in HJ-DGV-TFETs and make a contribution to the wider discussion surrounding the direction of semiconductor technology.

PROPOSED DEVICE ARCHITECTURE

The HJ-DGV-TFET, as shown in Fig. (**1**), is the configuration used in this study. InP serves as the source material for this device, and In0.47Ga0.53As serves as the channel/drain material. Because the InGaAs channel and InP source materials are combined, the tunnel junction formed is hetero-structured. HfO2, which has a dielectric constant value of 22, is chosen as the gate material dielectric. The two materials that comprise the gate materials are gate material 1, which has a work function of 4.1 eV, and gate material 2, which has a higher value of 4.3 eV. Notably, in order to minimize ambipolar current, the source section has a higher doping concentration than the drain section.

The tool TCAD Sentaurus is used to simulate the device structure. To simulate the tunneling phenomena, the model nonlocal path BTBT (band-to-band tunneling) is used. Fig. (**4**) depicts the correlation between the drain current (Ids) and the input gate-to-source voltage (Vgs) with respect to the drain-source voltage (Vds). The device performs best at Vds=0.5V, with a higher ON current of 2.63×10-5 A/µm and an OFF current of 2.74×10-13A/µm. This is impressive. The outstanding ON/OFF current ratio of 1.1×108 is produced as a result. Table **1** gives the values for the various device design limitations that were used based on the ITRS [1] specifications to achieve the best possible performance for the HJ-DGV-TFET. Similarly, the configurations of the Hetero Buried Oxide HJ-DGV-TFET (HBHJ-

CHAPTER 5

Novel Tunnel Field Effect Transistors

P. Suveetha Dhanaselvam[1,*], B. Karthikeyan[1], K.M.D Sridharshan[1] and **C. Muthu Pandian[1]**

[1] *Department of ECE, Velammal College of Engineering and Technology, Madurai, Tamil Nadu, India*

Abstract: This research aims to explore the complex challenges regarding reliability and scalability in Heterojunction Dual Gate Vertical Tunnel Field Effect Transistors (HJ-DGV-TFET). Specifically, it focuses on comparing the hetero buried and stacked buried configurations. The study thoroughly examines factors affecting reliability, such as traps, noise susceptibility, lateral straggle, self-heating, and scalability effects. These factors collectively impact the performance and lifespan of advanced electronic devices. Through extensive simulations under different operational conditions, this investigation quantifies and compares the influence of these reliability issues in both configurations. Additionally, the study delves into how HJ-DGV-TFETs maintain their reliability as technology continues to scale down.

Keywords: Hetero buried oxide, HJ-DGV-TFET, Noise, Oxide thickness, Stacked buried oxide, Source doping, Traps, Temperature variations.

INTRODUCTION

Novel devices with an operational concept distinct from MOSFETs have emerged to address the issues in MOSFET scaling and offer new possibilities in nanoelectronics. TFETs work on the basis of inter-band tunneling, exhibiting negligible short channel effects (SCEs), reduced leakage current, and a sub-60 mV/dec subthreshold swing (SS). Because of their desirable behavior, TFETs can be used in CMOS technology as an alternative to conventional MOSFETs [1-4]. There is movement of charge carriers for both positive and negative gate bias due to its ambipolar nature, which has severe implications for applications utilizing digital circuitry. To maximize TFET performance, researchers are continually looking at new material developments, device topologies, and fabrication methods.

*** Corresponding author P. Suveetha Dhanaselvam:** Department of ECE, Velammal College of Engineering and Technology, Madurai, Tamil Nadu, India; E-mail: suveethaj@gmail.com

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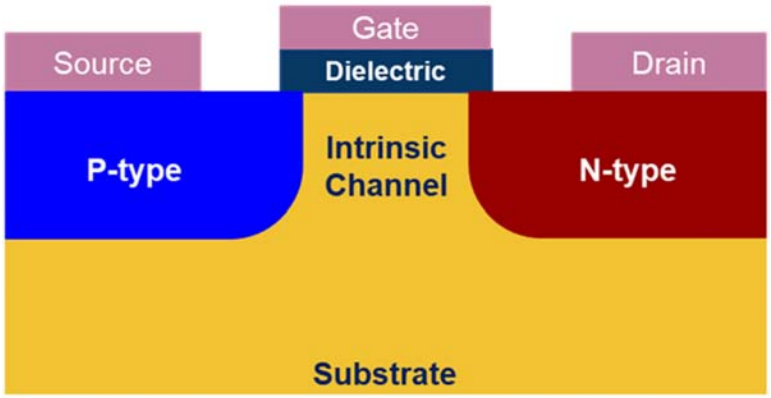

Fig. (1). Structure of TFET.

TFET functions using the principles of quantum tunneling and its schematic diagram are shown in Fig (**1**). This substitute for conventional MOSFET technology aims to tackle some drawbacks of MOSFETs, especially concerning power consumption. TFETs feature source and drain regions, much like MOSFETs do. The thin intrinsic channel area is sandwiched between the heavily doped n-type drain and p-type source. The charge carrier flow across the channel is effectively controlled by the gate terminal. In a MOSFET, both the source and drain are typically heavily doped with the same type of dopant (n-type for NMOS and p-type for PMOS). Current flows when a gate voltage is applied, and carriers move between the source and drain. In TFET, the source is heavily doped with the opposite type of dopant as compared to the drain. For example, in an n-type TFET, the source is p-doped, and the drain is n-doped, as shown in Fig. (**1**). This p-n junction is critical for enabling the tunneling mechanism. The classic TFET has garnered recognition for its intrinsic attribute of low power consumption. Yet, its efficacy is tempered by inherent limitations such as low ON-current and complexities in fabrication processes. To surmount these challenges, a spectrum of TFET variants has emerged, each distinguished by novel architectures, material compositions, and geometric configurations [5].

Vertical and nanowire TFETs represent seminal advancements aimed at augmenting tunneling efficiency. By redefining transistor architecture through vertical alignment or harnessing nanowires as conduits for charge carriers, these innovations significantly bolster operational performance, offering a ray of optimism amid the prevailing constraints. Similarly, heterojunction TFETs leverage disparities in bandgap characteristics to navigate the terrain of limitations, indicating a promising trajectory for further exploration. In the pursuit of streamlined functionality without compromising efficiency, junctionless TFETs emerge as paradigms of efficiency. By circumventing the particulars associated with conventional junction formation, these devices streamline fabrication methodologies, thereby facilitating greater accessibility and scalability. Junctionless TFETs cater to the demands of sensitive applications, where precision and reliability are paramount.

TFET VARIANTS

Lateral TFET

Lateral TFETs feature a horizontal channel architecture, where the current flows horizontally over the semiconductor substrate. This design offers advantages such as reduced short-channel effects and enhanced electrostatic control. The unique feature of lateral TFETs lies in their ability to exploit quantum tunneling phenomena, enabling charge carriers to traverse from source to drain more efficiently under the influence of an applied gate voltage, thus creating an electric field in the channel region. The simulated transfer characteristics of the Lateral FET are depicted in Fig. (**2**). These characteristics were obtained by varying the gate voltage from V_{GS} = 0.1 V to 1.5 V while keeping the drain-source voltage (V_{DS}) constant at 1.0 V [6].

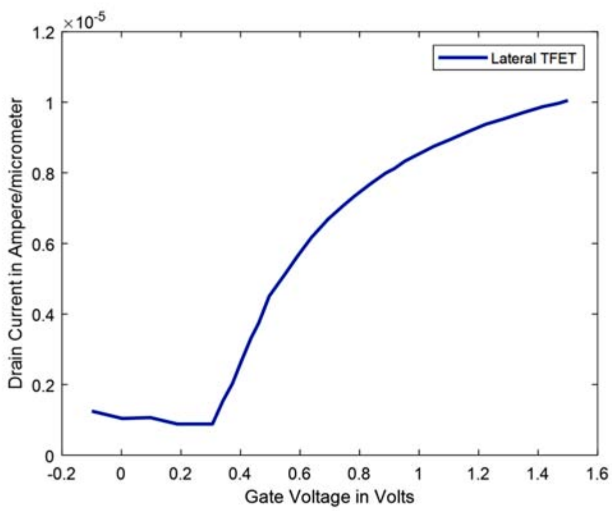

Fig. (2). I-V Characteristics of Lateral Tunnel FET.

This mechanism grants lateral TFETs a high subthreshold slope, allowing them to operate at exceptionally low power levels while exhibiting effective switching behavior. Thus, lateral TFETs are particularly well-suited for applications requiring

CHAPTER 6

DC/RF and Intermodulation Distortion Analysis of Hetero-Gate-Dielectric Double Gate TFET

Ashish Kumar Singh[1], **Ramesh Kumar**[1,2,*], **Shivalika Sinha**[2], **Satyabrata Jit**[1], **Sunil Dhawan**[1] and **Vikas Malhotra**[1]

[1] *Department of Electronics and Communication Engineering, Chitkara University Institute of Engineering and Technology, Chitkara University, Punjab, India*

[2] *Department of Electronics Engineering, IIT (BHU), Varanasi, UP, India*

Abstract: Purpose- In this manuscript, we have simulated a TFET device of the name hetero-gate dielectric tunnel field effect transistors with a source pocket (PHGD-TFET) of 5nm length in a channel on the source side. Therefore, our proposed device can be used for low-power applications. Design/Methodology Approach- We have compared all the DC/RF and linearity analysis parameters with simple gate hetero dielectric tunnel field effect transistors (HGD-TFET) by taking all other parameters the same. The structure simulation was done through the ATLASTM TCAD tool. The tunneling of extra carriers from the source to the channel region is the fundamental physics of the event. Finding- The subthreshold swing of our proposed device is 15 mV/dec, which is nearly four times lower than basic HGD-TFET, so it can be used for low-power applications. The ON-state current is increased by inserting a pocket in the channel region on the source side but has very little effect on the OFF current; therefore, PHGD-TFET is a more sustainable and energy-efficient device. Originality/value. In this work, we have designed our own structure of TFET with new dimension values and parameters.

Keywords: Tunnel field effect transistor (TFET), Hetero gate dielectric, Band-to-Band-tunneling (BTBT).

INTRODUCTION

As we move to manufacture low power and additional vitality productive devices alongside scaling channel length, off-current present and reserve control dissemination are becoming serious issues. The power supply drops as MOSFETs are scaled down [1]. It becomes crucial to lower the subthreshold swing (SS) and restrict the MOSFET SS (to 60 mV/dec) at room temperature in order to retain a high current while minimizing leakage current [2]. Due to low values of

* **Corresponding author Ramesh Kumar:** Department of Electronics and Communication Engineering, Chitkara University Institute of Engineering and Technology, Chitkara University, Punjab, India;
E-mail: rameshkumarmeena@gmail.com

subthreshold swing (*SS*<60 mV/dec), TFET is a low-power device [3]. It is hard proportional to the MOSFET supply voltage without significantly expanding the OFF-state current [4]. The majority of CMOS-based transistors (such as Bulk, Fin-FET, and completely depleted silicon-on-separator (CDSOI)) seem to show SS values of at least 60 mV/dec (2.3 kT/q) at room temperature, while the impact-ionization MOS-based transistor (IMOS), carbon nano tube-based tunnel FET (T-CNFET), and nanowire FET (NWFET) have lower SS values [4]. Recently, to overcome short channel effects, an alternative structure has been proposed in MOS based device known as TFET. The TFET operates much like a gated p+-i-n+ diode when reverse-biased. The band-to-band tunneling (BTBT) field-effect transistor (TFET) is a noteworthy device mainly because of its ability to create a steep sub-threshold slope and extremely low OFF-state current (I_{OFF}) [5]. However, due to the limited tunneling probability in doped Si junctions, almost all Si-based TFETs display a low On-current (I_{ON}). TFETs can contest the conventional MOSFETs due to their outstanding subthreshold features, abridged short channel effects, and low OFF-state current [5].

Improving TFET ON-state current without sacrificing OFF-state current is one of the main research issues in this area [6]. In this paper, we have used a pocket at the source channel interface, which has improved all the DC and RF parameters of the device. We have also used gate dielectric engineering in this device, which is responsible for increasing the conduction current [7].

The present work deals with device physics, design, and optimization of improved hetero gate dielectric pocket TFET and heterojunction double gate TFET. We have investigated the influence of different device structural parameters, such as the k-value of the gate oxide, width of the spacer, source and drain doping concentration value, *etc*. The device performance of a TFET is investigated on p-channel devices. A detailed investigation has been carried out to find the current saturation mechanism in the given TFET structures [7]. The aforementioned findings simplify the construction of a device framework appropriate for analog/mixed-signal system-on-chip applications. An analysis of the TFET's analog performance reveals a respectable drain current at saturation. Different device parameters for analog applications are studied for the Improved Hetero-Gate-Dielectric Pocket TFET and Heterojunction-Double-Gate TFET. In order to achieve high performance, high I_{ON}, low I_{OFF}, and low subthreshold swing (SS) with lower power consumption, Modified Hetero-Gate-Dielectric TFET is the most promising device. We have achieved an ON-state current of 5.38×10^{-5} A/µm, I_{ON}/I_{OFF} of 6.59×10^{10}, SS of 15 mV/dec, and a maximum cut-off frequency of 400 GHz [8].

The implementation of an ultra-steep doping profile at these junctions, however, is very challenging and expensive [9]. Multi-gate devices called junction-less transistors have been proposed as a way to get around the short-channel devices' high thermal budget restriction. Diffusion across these locations is not possible in JLT because the gradient in doping concentration between the source, channel, and drain is zero. Diffusion cannot thus occur between these locations. Consequently, the need for the expensive millisecond annealing process is no longer necessary [10, 11]. As is well knowledge, junctionless devices have less short channel effects since there is no depletion layer present. Due to its extremely thin body, JLT has a lower ON current than conventional MOS. Better gate control over the channel is achieved by using a thin body [12, 13]. A lower ION to IOFF ratio due to a smaller JLT ON current compromises the functionality of the device. In addition, because there are no junctions, oxidation and lithographic complexity are reduced, making JLTs much easier to fabricate [14].

The leakage current has grown worse because MOSFETs continue to scale. The reverse-biased pn junction that is created between the source and bulk and the drain and bulk causes the most leakage [15]. Because there are no metallurgical connections in junctionless devices, this leakage is considerably reduced. Tunneling from band to band is the primary source of leakage in JLT [16]. A better knowledge of leakage reduction in JLTs is provided by the thorough examination of leakage in devices with junctions and without junctions. The conduction band and the valence band overlap at the point where the drain extension meets the channel in order to effectively manage the channel electric field [17]. This causes BTBT of electrons from the channel to the drain, significantly increasing OFF state leakage current [18].

Additionally, a drop in oxide thickness leads to an increase in the electric field across the oxide layer, which may cause electrons to tunnel through the oxide layer [19, 20]. A bidirectional way from a negative gate voltage to the gate substrate and from the substrate to the gate for a positive gate voltage is capable of tunneling through this thin oxide. There are six main forms of leakage currents and other factors in MOSFETs [21, 22]. Sub-threshold leakage, tunneling through gate oxide, tunneling types, effects, and leakage resulting from BTBT of electrons have all been reported to be substantial in junctionless transistors [23, 24].

Leakage Current in Conventional

These are leakage currents *via* p-n junctions with reverse bias. Subthreshold at the source/drain bulk interface leakage is due to tunneling *via* gate oxide, gate leakage

CHAPTER 7

Dual Pocket Step Channel TFET for Improved Low-Power Performance

Abhinav Rajyan[1,*] and **Gaurav Saini**[1,2]

[1] *Department of Electronics and Communication Engineering, School of VLSI Design and Embedded Systesm, NIT Kurukshetra, Haryana, India*

[2] *Department of ECE, NIT Kurukshetra, Haryana, India*

Abstract: In this chapter, we introduce a novel Tunnel Field-Effect Transistor (TFET) structure explicitly engineered for low-power applications. The proposed TFET structure offers an improved ION/IOFF current ratio and reduced subthreshold swing values, making it highly suitable for energy-efficient electronic devices. The design achieves a stepped channel by incorporating drain underlapping and channel engineering techniques, effectively reducing ambipolarity current. The proposed structure outperforms conventional TFETs with a 71% smaller average subthreshold swing (SS), demonstrating enhanced efficiency. These improvements address the demand for energy-efficient devices in fields such as portable electronics and the Internet of Things (IoT), demonstrating the innovative TFET structure's potential for low-power applications.

Keywords: CTFET, DPSC-TFET, Non-local BTBT model, Screening length.

INTRODUCTION

Advancements in technology driven by the pursuit of upholding Moore's Law have led to the scaling down of integrated circuits (ICs), resulting in improved operating speed and packaging density. However, this reduction in size has brought forth challenges, particularly in deep-sub-micrometer regimes, in the form of high leakage current, which leads to excessive power dissipation in CMOS circuits [1, 2]. CMOS technology has become popular in digital circuit design due to its excellent performance, reliability, affordability, and minimal power consumption during standby [3]. As device miniaturization persists, MOSFET-based devices face short-channel effects. These effects pose significant challenges, including a decrease in threshold voltage, increased drain-induced barrier lowering, and various other factors that impede transistor functionality. As the dimensions of devices

*** Corresponding author Abhinav Rajyan:** Department of Electronics and Communication Engineering, School of VLSI Design and Embedded Systesm, NIT Kurukshetra, Haryana, India;
E-mail: rajyanabhinav1@gmail.com

continue to shrink, the impact of these effects becomes increasingly pronounced, necessitating innovative strategies to mitigate their adverse consequences and uphold optimal transistor performance. These effects become more pronounced as the dimensions of the transistor decrease, which is a common trend in the electronics industry as manufacturers strive to make devices smaller and more efficient. including increased leakage current [4-8]. Decreasing MOSFETs' threshold and supply voltage beyond a certain point has implications for energy efficiency. There's a restriction on the subthreshold swing (SS), which must be at least 60 mV/dec at room temperature [7].

Researchers have investigated alternative operational principles in the pursuit of devices exhibiting subthreshold swing values below 60 mV/dec. Among these alternatives, the TFET has emerged as a promising candidate, offering potential solutions to the limitations associated with subthreshold swing while demonstrating capabilities for ultra-low leakage currents [8]. The TFET, characterized by its distinct transistor type, operates through a gated reverse-biased p-i-n device structure. It facilitates current conduction by leveraging inter-band tunneling of charge carriers across barriers rather than relying on thermal diffusion over the obstacles [9, 10]. While TFETs share construction similarities with MOSFETs, the key distinction lies in the opposing doping of the source and drain regions. Tunnel Field-Effect Transistors (TFETs) operate based on the principle of quantum mechanical tunneling, which sets them apart from traditional MOSFETs. In a TFET, when a voltage is applied to the gate, it creates a strong electric field that lowers the energy barrier between the source and the channel. This barrier reduction allows electrons to "tunnel" through the barrier from the source into the channel, even at lower gate voltages. Unlike conventional MOSFETs, which rely on the movement of charge carriers over a barrier, TFETs exploit this tunneling effect to enable current flow. This mechanism allows TFETs to achieve efficient operation and switching at much lower voltages, significantly reducing power consumption. However, TFETs have faced challenges in achieving commercially viable on-current (I_{ON}) levels [11]. In response to the challenge of low I_{ON} in TFETs, numerous innovative TFET designs have been reported in scientific literature. These designs aim to address and overcome the limitations by introducing novel device structures, incorporating high-k gate dielectrics, and optimizing parameters such as gate dielectrics and gate length scaling. High dielectric constant (k) allows for a thicker layer that reduces leakage current while still maintaining the same capacitance as a thinner layer of traditional silicon dioxide. This is crucial as device dimensions shrink in accordance with Moore's Law. The metal gate is used in conjunction with the high-k dielectric [12].

Traditional polysilicon gates suffer from the ‘poly depletion effect,’ which effectively reduces the gate capacitance. A metal gate does not suffer from this effect and thus maintains the full capacitance of the gate stack. The combination of high-k dielectric and metal gate allows for continued scaling down of transistor dimensions, improving performance and reducing power consumption. However, this technology presents challenges stemming from various sources. These include the threshold voltage variability induced by random dopant fluctuations, which arise from the inherently stochastic nature of dopant placement during fabrication. Additionally, concerns regarding reliability have surfaced, encompassing aspects such as device longevity and consistency of performance over time. Furthermore, issues pertaining to process integration have been identified, referring to the complexities involved in seamlessly incorporating this technology into existing manufacturing processes [13]. The objective is to achieve enhanced subthreshold swing, I_{ON}/I_{OFF} ratio, and overall device performance, thereby facilitating efficient operation in low-power and high-speed applications, ultimately resulting in increased I_{ON} [14-16].

One notable advancement is the introduction of a novel device structure known as step channel Tunnel FETs (SC-TFET). SC-TFET is specifically engineered to overcome the constraints observed in conventional TFETs [17]. It accomplishes this by boosting the ON-state current, mitigating ambipolar behavior [18], and enhancing subthreshold swing through strategic variations in dielectric thickness at the source/drain-channel junctions. Furthermore, an innovative high-k dielectric material is integrated as an oxide layer, termed high-k SC-TFET, which further amplifies the I_{ON} performance [19].

In the proposed device, we have significantly increased the on-current (I_{ON}) by strategically implementing gate-source overlap at the source end. This design enhancement optimizes gate control over the channel, facilitates efficient carrier injection from the source, reduces source resistance, and promotes a broader channel conduction region. These improvements enhance the device's current-carrying capacity in the 'on' state, making it well-suited for applications demanding higher current levels and superior performance.

Furthermore, Tunnel Field Effect Transistors (TFETs) traditionally face challenges such as increased off-state current (I_{OFF}) due to channel-length scaling beyond certain limits and larger gate-to-drain ('Miller') capacitance, which can impact circuit design. To address these issues, our proposed device incorporates gate underlap, modifying the electric field distribution, particularly at the drain side of the channel. This modification reduces the lateral electric field strength in the

CHAPTER 8

Analysis of Transition Metal Dichalcogenides-Based TFET

Priya Kaushal[1,*] and **Gargi Khanna**[1]

[1] *Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur, Himachal Pradesh, India*

Abstract: This article describes in detail Tunnel Field-Effect Transistors (TFETs) that are based on Transition Metal Dichalcogenides (TMDs). TFETs have garnered significant attention due to their potential for low-power electronics. Leveraging the unique properties of TMDs, including tunable bandgaps and high carrier mobilities, holds promise for enhancing TFET performance. The study explores the impact of TMDs on TFET characteristics, focusing on parameters such as bandgap engineering and current enhancement. Performance metrics of the device, such as subthreshold slope (SS), threshold voltage (Vth), on-state current (Ion), off-state current (Ioff), and Ion/Ioff ratios, are evaluated through comparative analyses of diverse channel materials, including MoS2, MoSe2, MoTe2, WS2, and WSe2. The research findings obtained from this analysis illuminate the possibility of TMD-based TFETs in the progression of low-power electronics and provide significant recommendations for further optimizing devices and investigating applications.

Keywords: 2D material, Transition Metal Dichalcogenides (TMD), Thickness Engineered, Tunnel Field Effect Transistor (TFET).

INTRODUCTION

In response to the growing need for more compact, efficient, and functional integrated circuits, CMOS devices have experienced a progressive reduction in dimensions. One problem with this shrinking is that CMOS technology loses a lot of power, especially in devices smaller than 100 nm. This power loss is caused by increased leakage current and the requirement for a broad supply voltage range in MOSFETs [1-3]. The leakage current is significantly intensified by Short Channel Effects, a concern that can be mitigated to some extent by employing novel transistor designs. Another option is to increase the supply voltage to get a larger drive current and quicker operation. For a transistor to have a low SS, which enables

*** Corresponding author Priya Kaushal:** Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur, Himachal Pradesh, India; E-mail: priya@nith.ac.in

rapid transitions between the off and on states, the supply voltage of the transistor must be decreased without sacrificing its performance. Although at room temperature, the lowest attained SS for semiconductor devices is only 60 mV per decade, which is far greater than what is intended for functional nanoscale transistors. Alternative FETs with very low SS are being researched as a result of the shortcomings of present nanoscale MOSFETs [4-6]

The TFETs have become more popular than the nanoscale MOSFETs because of their special carrier injection method, called BETT. With this method, leakage current may be reduced to 60 mV per decade, paving the way to device downsizing. On the other hand, TFETs encounter difficulties because the on-state current (I_{on}) and charge transfer are both impacted by the band-to-band tunneling (BTBT). TFETs have a much lower I_{on} than typical transistors, highlighting the need to optimize device design and materials. The investigation of TFETs at both the theoretical and design levels has become an increasing area of research emphasis in the last decade. Numerous techniques have been developed to improve TFET performance, with the choice of semiconductor materials emerging as a significant factor. In addition to addressing TFET-related issues, this ongoing study hopes to enhance semiconductor technology [7-12]

Before delving into 2D semiconductor materials, it is essential to first clarify the advantages they offer over traditional silicon-based materials. 2D semiconductors, such as graphene and transition metal dichalcogenides (TMDs), are composed of only a few atomic layers, allowing for unprecedented miniaturization in electronic devices, something silicon cannot achieve without losing its functionality. Additionally, these materials exhibit superior electrical properties, such as higher electron mobility, which enables faster and more energy-efficient devices. Unlike silicon, 2D semiconductors also offer tunable bandgaps, which are crucial for creating low-power, high-performance transistors and optoelectronic devices. Their flexibility allows for strain engineering, where electronic properties can be adjusted by stretching or compressing the material, a feature that is difficult to replicate in silicon. Furthermore, 2D materials can perform well at the nanoscale, where silicon faces limitations like heat dissipation and leakage currents. Lastly, their transparency and flexibility make them ideal for innovative applications such as flexible electronics, transparent solar cells, and wearable technology, areas where silicon falls short. Understanding these advantages is key to appreciating why 2D semiconductors hold such promise for the future of electronics [13-16].

Since 2004, when the first graphene was made, a lot of work has been done on two-dimensional (2D) semiconducting materials that are made up of only a few atomic layers. Due to significant quantum mechanical effects, limited particle scattering events, and improved correlations, this growing class of 2D materials reveals unique physical characteristics. These 2D materials have extraordinary optical, magnetic, and electrical properties, which distinguish them from their 3D bulk counterparts. Furthermore, developments in synthesis processes enable the continuous and controlled manufacture of high-quality 2D materials with layers as thin as a single atomic layer on a variety of substrates [17-22]. On the other hand, the integration of TMDs over graphene holds immense promise for advancing nanoelectronics and optoelectronics. TMDs, with their tunable bandgaps and unique electronic properties, when deposited onto graphene, leverage the latter's exceptional conductivity and mechanical strength. This combination offers a versatile platform for developing high-performance devices, ranging from transistors to photodetectors. By exploiting synergistic interactions between TMDs and graphene, researchers can engineer heterostructures with tailored electronic properties, paving the way for innovative applications in next-generation electronics and photonics [23-28].

Theoretical research using computational nanomaterials approaches, particularly first-principles calculations employing density functional theory (DFT), has significantly contributed to the advancement of acquiring information regarding the basic physical properties related to these nanostructured materials. This computational approach successfully complements experimental findings and has contributed to the successful development of electrical, optoelectronic, and spintronic devices based on 2D materials, often exhibiting superior performance compared to bulk materials. In the realm of FETs, 2D materials are currently a subject of extensive exploration. Due to a greater surface-to-volume ratio, 2D transistors provide advantageous electrostatic control over the gate electrode, improved electrical conductivity *via* ballistic movement, and an optimal surface area that ensures enhanced structural interactions with insulators [29-35]. Additionally, the tunable electrical properties based on layer and stacking configurations provide flexibility in transistor design. As channel materials for FETs, 2D materials are particularly promising. Their incorporation into transistors for TFETs holds the potential to harness benefits such as increased electrostatic stability and the engineering of tunneling barriers. Over the past years, the use of TFETs with 2D materials as channel materials has seen significant growth, especially in nano-device applications with channel lengths around 40 nm, resulting in ballistic carrier movement in the channel. However, the implementation of nanoscale 2D TFETs requires careful consideration of specific design aspects due to the significantly altered device physics at such scales. Notably, advancements in device/material co-optimization have been achieved, involving diverse techniques

CHAPTER 9

Performance Analysis of AlGaN/GaN HEMTs

P. Suveetha Dhanaselvam[1,*], Subashi S.[1], Vasunthra R.S.[1] and **G. Annam[1]**

[1] *Department of ECE, Velammal College of Engineering & Technology, Madurai, India*

Abstract: This chapter provides a comprehensive analysis of recent advancements and applications of High Electron Mobility Transistors (HEMTs), with a specific focus on AlGaN/GaN-based technologies. Various aspects of HEMT performance and optimization strategies are explored through a series of studies, ranging from DC characteristics and low-frequency noise to statistical modeling of manufacturing variability and temperature-dependent large-signal modeling. Additionally, comparisons between different HEMT configurations and materials are presented, highlighting their respective strengths and applications across different temperature regimes, including cryogenic temperatures and millimeter-wave frequencies. The synthesis of these findings underscores the continuous evolution and promising future of HEMTs in powering diverse electronic applications with enhanced performance, stability, and efficiency.

Keywords: High Electron Mobility Transistors (HEMTs), AlGaN/GaN-based technologies, DC characteristics, low-frequency noise, statistical modeling, manufacturing variability, temperature-dependent modeling, performance optimization, cryogenic temperatures, millimeter-wave frequencies.

INTRODUCTION

In the nanoscale era, High-Electron Mobility Transistors (HEMT) have demonstrated the extraordinary potential of the two-dimensional electron gas (2DEG) in III-V semiconductors, opening new avenues for significant developments in electronics [1]. HEMTs have changed dramatically in the last forty years as new and improved materials have been investigated and developed to improve their functionality [2]. AlGaAs/GaAs and AlGaN/GaN combinations have proven to be the most effective among these materials, providing a special blend of high power, quick operation, and low noise. The unique combination of high power, fast operation, and low noise makes GaN-based HEMTs a particularly interesting material among these materials. They also have the potential to be the most effective at high voltage. GaN-based HEMTs are one area of special interest as they have great potential for high-voltage power regulation and the developing field of

*** Corresponding author P. Suveetha Dhanaselvam:** Department of ECE, Velammal College of Engineering & Technology, Madurai, India; E-mail: suveethaj@gmail.com

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6G technology. This research explores several modeling and analysis approaches [3].

Defects' trapping effects in AlGaN/GaN HEMTs restrict the functionality and dependability of the device [4-6]. It examined and contrasted the noise spectrum and DC current-voltage characteristics. Gate positions of AlGaN/GaN HEMTs are diverse between the source and drain. High Electron Mobility Transistors (GaN HEMTs) based on gallium nitride have become the preferred technology for power amplifier design in a variety of applications [5-7]. Statistical models can be utilized by designers to guarantee the necessary specifications, even in manufacturing deviations [1]. The ML algorithm determines the relationship between electrical and process parameters without taking device physics into account. This method has only been demonstrated for V_{OFF} [8].

The Machine Learning method complexity rises with the addition of more electrical parameters, making circuit simulations more challenging. They created an accurate statistical model of GaN HEMTs that takes into account changes in transistor processing by utilizing the industry standard physics-based ASM-HEMT model [9-10]. The impact of the gate dielectric on small-signal RF performance has been a topic of discussion among Schottky-gate HEMTs (SG-HEMTs) and Metal-oxide Semiconductors (MOS-HEMTs). Similar AlGaN/GaN structures using the same process method are compared for their microwave gain characteristics [11]. The MOS-HEMTs' characterization resulted in significant gains in small-signal gain. The design of monolithic microwave integrated circuits (MMICs) for high-temperature applications is confronted with a number of challenges.

Hypersonic vehicles, deep-well oil drilling, and space exploration are a few examples of HT applications [12]. Because of their large bandgap and low carrier heat degradation, gallium nitride (GaN) HEMTs are a good contender for semiconductor technology that can survive these harsh environments [13-14]. For the first time in their history, they provide a temperature-scale GaN HEMT model that accurately reproduces large-signal responses at high temperatures. GaN-HEMTs showed competitive low-noise operation capability at cryogenic temperatures [5]. The contribution of gate insulation to the low-noise amplifier (LNA) design at room temperature was examined in terms of low-noise performance [15].

The polarization gradient produces a three-dimensional electron "slab" for the channel rather than a two-dimensional electron gradient when it grades the channel compositionally in the vertical (growth) direction [16]. The research provides a thorough analysis of graded-channel devices' functioning to clarify these findings. The channel noise temperature and noise statistics may be influenced by the lateral electric field. These investigations aid in the explanation of the fundamental physics of graded-channel GaN-powered gadgets [17].

The P-GaN Gate HEMT device structure (Fig. **1**) is the one that has been the most extensively studied among the various technological approaches. It has proven to be reliable in a wide range of industrial applications, supports E-mode operation for single-chip enhancement, and allows for the fabrication of large-scale power integrated circuits. This work shows the dynamic stability of a newly built enhancement-mode (E-mode) active-passivation p-GaN gate HEMT (AP-HEMT), as shown in Fig. (**1**). Because of the active passivation layer, the rearranged electric field distribution effectively suppresses the dynamic OFF-state leakage of the AP-HEMT [18]. E-mode active-passivation p-GaN gate HEMTs are advanced transistors used in high-frequency and high-power applications, particularly in power electronics. These E-mode devices are normally off, requiring a positive gate voltage to conduct, which offers safer operation compared to depletion-mode (D-mode) HEMTs. A thick layer of GaN is grown on the sapphire substrate to provide a high-quality surface for the subsequent layers. A thin layer of aluminum gallium nitride (AlGaN) is grown on the buffer layer. This layer creates a potential well at the interface with the GaN channel.

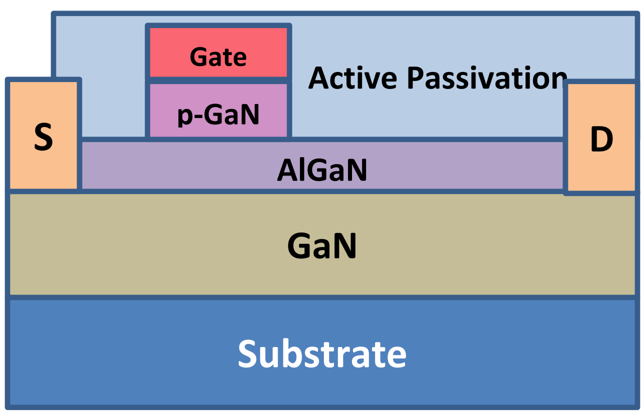

Fig. (1). Schematic cross-sectional structure of the active passivation p-GaN gate HEMT.

The p-GaN gate structure, incorporating a p-type gallium nitride layer, provides a built-in positive threshold voltage, enabling normally-off operation without the need for large negative gate voltages, thus simplifying circuit design. In a P-GaN gate HEMT with active passivation, the passivation layer is typically deposited on

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Dharmendra Singh Yadav

Dharmendra Singh Yadav received the Ph.D. degree in Electronics and Communication Engineering from the PDPM-Indian Institute of Information Technology, Design and Manufacturing , Jabalpur, India. After Completing Ph.D., he joined as an Assistant Professor and is currently serving in the Electronics and Communication Engineering Department, as a faculty member at National Institute of Technology (NIT), Kurukshetra, Haryana, India. He has more than 70 international publications and 6 book chapters. His current research interest includes VLSI Design: Nano-electronics Devices, Thin films transistors, Semiconductor Device, Negative Capacitance, Nanosheet FETS and circuits. Device Modeling: MOS Devices Modeling and Numerical simulation analysis of Semiconductor devices Electrical Characterization of semiconductor devices in MHz and THz frequency ranges. Circuit Design: Ultra Low Power SRAM / DRAM / RRAM based Memory Circuit Design from Devices to Array Architecture using CMOS and Advanced CMOS Devices technologies. Machine Learning in Semiconductor device/circuit-based application in research.

Prabhat Singh

Prabhat Singh received a B.E. degree from the Uttar Pradesh Technical University, India; M.Tech. degree in Electronics and Communication Engineering from the Dr. B. R. Ambedkar National Institute of Technology, Jalandhar, India, Punjab; and PhD from the National Institute of Technology, Hamirpur, Himachal Pradesh, India. Dr. Prabhat Singh is post-doctoral research associate at IIT Bhubaneswar, Odisha. Dr. Prabhat Singh research revolves around different semiconductor devices including ultra-scaled FETs, solar cells, Quantum Dots, etc. and their prospective applications. He is currently working on unravelling the interfacial behavior of different FET based biological sensors using different classical and semi-quantum analytical models. He has authored/co-authored more than 20 research articles/ papers in leading peer reviewed international journals and conference proceedings. He has more than 5 book chapters to his credit. His main areas of research interest include semiconductor device physics, solid-state devices, analog complementary metal oxide semiconductor (CMOS) integrated circuits, nanoscale device design and simulation, etc.