NANOELECTRONIC DEVICES AND APPLICATIONS

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Nanoelectronic Devices and Applications

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PREFACE

Nanoelectronic devices play a crucial role in current and future practical applications, including quantum computing, automotive, display, sensing, high-power electronics, and consumer electronics. These emerging applications have their specific, unique requirements and demand integration of functionalities into a single chip with high efficiency, smaller size, lightweight, and high-power handling capability. These research fields have attracted researchers and are of great interest in the photonic and electronic communities.

This book contains 16 chapters, presenting recent advances as well as new directions in emerging nanoelectronic devices and their applications. It covers novel materials systems, band engineering, theoretical calculation, modeling and simulations, fabrication and characterization techniques, and emerging applications of nanoelectronic devices. Several discussions presented in this book are based on current innovations and trends toward the next several years.

Chapter 1 presents an overview of recent innovations and future prospects in III-nitride semiconductor technologies for RF, power, digital and quantum computing applications.

Chapters 2 and 3 report new trends in GaN-based optical devices for sensing and micro-display applications. In Chapter 2, a comprehensive review on GaN-based sensors is presented, and a special focus is on GaN-based integrated optical devices with detailed elucidations on their sensing mechanisms, device fabrication, performance, and applications. Chapter 3 shows current interests in nanophosphors and their utilizations in improving the device performance of InGaN nanowire light-emitting diodes (LEDs). These approaches provide potential solutions for achieving high efficiency micro-LEDs for micro-display, AR/VR headset applications.

Recent studies on the effect of potential profile on the carrier transport in AlGaAs-based double quantum well structures and their applications are explained in Chapter 4. This chapter lists possible approaches for the improved performance of emerging low dimensional semiconductor devices by engineering their band energy structures.

Recent progress in high-electron-mobility transistors (HEMTs) is presented in Chapters 5, 6, and 7. Current developments, general challenges in device fabrication and reliability, and future prospects of HEMTs are also clearly discussed in Chapters 5 and 6. Chapter 7 shows the capabilities of the ADS tool in simulating the characteristics of HEMTs.

A comprehensive review of β-Ga_2O_3 with details on material properties, growth approaches, and its applications for next-generation high-power electronics is displayed in Chapter 8. This chapter also discusses the potential of this material system for future nanoelectronics. Looking at the different figures of merit for different ultrawide band gap semiconductors of interest, β-Ga_2O_3 material has the potential for far superior performance than conventional wide band gap semiconductors (GaN and SiC). Chapter 9 presents detailed investigations of the effect of dielectric layers on the characteristics of AlN/β-Ga_2O_3 HEMTs. These studies provide deep insight into the design and development of HEMTs for high-frequency and high-power electronic devices.

Chapters 10-14 summarize recent studies on field-effect transistors (FETs) adopting different materials and structures. Chapter 10 discusses the device performance based on electrostatic parameters in InAs raised buried Oxide SOI-TFET with n-type SiGe pocket. The tunneling

width and the lateral electric field play important roles in the subthreshold swing of the devices. Chapter 11 summarizes current approaches to achieve high-performance ETLTFET compared with its homo-junction counterpart by using SiGe source-based epitaxial layer-encapsulated TFET. Chapter 12 includes important studies for reducing the effect of trap charges on numerous electrical properties in traditional NR-FETs by using heterodielectric BOX nanoribbon FET structures. These studies show important approaches to the design of high-reliability TFET. Chapter 13 discusses a unique configuration of FET using nanosheet FinFET structures. The design, operation, device performance and emerging application of this type of FET are presented in this chapter. The applications of FET and HEMT have been intensively investigated for biosensing applications, including label-based and label-free detection techniques. Chapter 14 presents recent trends in biosensors for medical diagnosis using FETs and HEMTs.

Chapter 15 summarizes current research on the 2-dimensional material Tungsten Diselenide (WSe_2) with a special focus on the material properties, device structures, applications, and challenges.

Chapter 16 presents a systematic review of in-demand applications of memristors and memristive semiconductor devices. Memristors show promising applications in neuromorphic and memory-remembering applications. Moreover, memristors are highly promising for the design of signal processors, FPGAs, and sensors. The theory, applications, and future perspectives of memristors for the silicon post-silicon era are clearly discussed.

We would like to take this opportunity to thank all authors for their valuable contributions to this book. We would also like to acknowledge all reviewers of this book for their time and comments.

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CHAPTER 1

Advancements in GaN Technologies: Power, RF, Digital and Quantum Applications

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Abstract: Quantum well devices based on III-V heterostructures outperform Field Effect Transistors (FETs) by harnessing the exceptional properties of the two-dimensional electron gas (2DEG) in various material interface systems. In high-power electronics, III-V-based Gallium Nitride (GaN) HEMTs can have a great influence on the transport industry, consumer, RADAR, sensing systems, RF/ power electronics, and military systems. On the other hand, the devices made of HEMTs and MIS-HEMTs work in enhancement mode, having very low leakage current, which can conserve energy for more efficient power conversion, microwave/ power transistors and high-speed performance for wireless communication. The existing physics of the well-established AlGaN heterostructure system imposes constraints on the further progress of GaN-based HEMTs. Some of the scopes include: Initially, the semiconductor materials made of SiC, GaN, and AlGaN allow a device that is resistant to severe conditions, such as high-power /voltage-high temperature, to operate due to its effective dielectric constant and has a very good thermal conductivity, which makes this device well-suited for military applications. Secondly, with the urgent need for high-speed internet multimedia communication across the world, high transmission network capacity is required. GaN-based HEMT devices are suitable candidates for achieving high-speed limits, high gain and low noise performance. In conclusion, GaN and related interface materials exhibit chemical stability and act as robust semiconductors, exhibiting remarkable piezoelectric polarization effects that lead to a high-quality 2DEG. Integrating free-standing resonators with functionalized GaN-based 2DEG formation reveals the potential for designing advanced sensors.

Keywords: AlGaN, GaN, SiC, Power devices and switching, III-V materials.

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INTRODUCTION

Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) exhibit a set of unique characteristics that make them increasingly attractive for high-frequency, high-power applications in the field of electronics. One of the key features of GaN HEMTs is their exceptional electron mobility, which allows for high-speed operation and efficient power handling. This characteristic, coupled with a wide band gap, contributes to their ability to operate at elevated temperatures without significant performance degradation. GaN HEMTs also have high breakdown voltage, enhancing their resilience to voltage spikes and enabling robust performance in power electronics applications. Furthermore, GaN HEMTs exhibit low on-resistance and parasitic capacitance, contributing to their efficiency and suitability for applications such as radio frequency (RF) amplifiers and power converters. The combination of these characteristics renders GaN HEMTs a promising technology for advancing the capabilities of electronic devices and systems in various industries.

In addition to their impressive electrical characteristics, GaN HEMTs offer notable advantages in terms of miniaturization and size reduction. Their inherent ability to operate at high frequencies enables the design of compact and lightweight devices, making them particularly well-suited for applications where space constraints are critical. GaN HEMTs also exhibit excellent power density, allowing for the development of more energy-efficient and power-dense electronic systems. The material's high thermal conductivity further enhances its performance, facilitating effective heat dissipation even in compact configurations. This combination of high-frequency operation, power density, and thermal management makes GaN HEMTs highly desirable for emerging technologies such as 5G wireless communication, radar systems, and satellite communications, where the demand for compact and efficient electronic components is paramount. As researchers and engineers continue to explore and optimize the potential of GaN HEMTs, their impact on advancing electronic capabilities across various applications is poised to grow significantly.

However, III-V GaN devices face hurdles in achieving E-mode operation with a positively biased threshold voltage (V_T) and finding a low-defect material interface with low OFF-state leakage. Advancements in power density, breakdown degradation modes, and operational capabilities have not been fully recognized yet, and these factors currently hinder the widespread commercialization of these devices in the market [1, 2, 3]. Hence, the primary objective is to achieve exceptionally high-performance GaN power devices capable of efficient power conversion and operation at high frequencies. This involves implementing enhancement-mode HEMT operation for fast switching

capabilities while simultaneously reducing switching losses to a minimum. Different performances need to be worked upon and are shown below:

• **OFF-state breakdown voltage ($V_{BR,OFF}$):** It needs to be over 1000 V, taking the surge capacity into consideration.

• **ON-state resistance (R_{ON})**: It should be as low as possible to minimize power loss, size and cost. Since a decrease in the ON-state resistance defines a reduction in the generation of heat inside devices, this makes cooling systems simpler, such as heat sinks, thereby making a significant contribution to the enhancement of efficiency and the development of simpler power supply circuits.

• **Normally-OFF**: Enhancement mode (E-mode) operation of the power switch allows for a simpler and more efficient design of the driving and control circuit.

Characteristics of GaN:

GaN is a semiconductor material that exhibits distinct characteristics, making it a compelling choice for a variety of electronic applications. One key feature of GaN is its wide band gap, which allows for efficient electron mobility and high-speed operation. This property makes GaN particularly suitable for applications requiring high-frequency switching, such as RF amplifiers and power converters. GaN devices also demonstrate a remarkable balance between high breakdown voltage and low on-resistance, contributing to their efficiency and reliability in power electronics. Additionally, GaN's excellent thermal conductivity allows for effective heat dissipation, enabling the design of compact yet high-performance electronic systems. The combination of these characteristics positions GaN as a crucial material for advancing technologies in areas like telecommunications, power electronics, and emerging fields such as electric vehicles and renewable energy systems.

Motivation for the Present Research Work

Investigations described in this work are motivated by the search for developing highly safe E-mode operation devices with positive V_T for low leakage and enhancing the OFF-state breakdown voltage and high-frequency operation in advanced III-V HEMT devices for the applications of efficient power-switching converter's/inverter's and low-noise amplifier's (*LNAs*) in microwave/RF systems. Although the technology is being studied since the early 1979s, there is still a vast room and expectations in its yet unachieved findings. The devices' performance remained restricted due to the effects of high-injection velocities and high-field nonlinearities, as discovered during the evaluation by Enrico Zanoni in 2013 [4]. Hence, to improve the devices' performance further, it is necessary to

CHAPTER 2

GaN-Based Integrated Optical Devices for Wide-Scenario Sensing Applications

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Abstract: Sensors that detect variations in the surroundings and convert them into electrical signals are crucial in numerous fields, including healthcare, manufacturing, and environmental monitoring. Optical sensors, in terms of various sensing principles, hold considerable potential due to their fast response, high sensing resolution, and ability to withstand magnetic interference. Despite their advantages, traditional optical sensing techniques also have certain limitations, such as bulky structures, tedious alignment procedures, and high production expenses. To address this issue, on-chip integration has been proposed, and GaN and its alloys can be ideal materials due to their high efficiency, long lifespan, and high stability. By simultaneously forming the light emitter and photodetector on a shared substrate through wafer-fabrication processes, miniaturized GaN optical sensors possess a compact design, small size, high robustness, low manufacturing cost, and simple operations. This chapter discusses the working mechanisms and influencing factors of integrated GaN devices alongside their recent progress in advanced sensing applications.

Keywords: GaN, Integrated optical devices, Optical sensors, Sensing devices.

INTRODUCTION

GaN semiconductors and their alloys have drawn extensive attention in the past few decades because of their remarkable thermal, electrical, and mechanical characteristics [1]. Thanks to the advancements in material growth and microfabrication techniques, numerous GaN-based structures and devices have been successfully designed and fabricated [2]. The rapid development of the Internet of Things has led to a surge in the demand for sensors in a variety of applications, and developing GaN-based devices that can sense environmental changes and convert them into electrical signals has become an important topic [3].

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In the past decade, high-electron-mobility transistors (HEMT) have been employed as one of the major types of GaN-based sensing devices. The device structure is shown in Fig. (**1a**). For HEMT-based sensors, an AlGaN/gate metal region is typically exposed as the sensing interface, beneath which lies a two-dimensional electron gas (2DEG) that governs the conductivity of the device. The effective sensing of gas, ions, and liquids is demonstrated by the interactions of the sensing substances with the exposed layer, which can change the barrier height, gate metal function, piezoelectrical polarization, and other parameters [4 - 6]. The properties of various semiconductors are shown in Table **1**.

Table 1. Properties of various semiconductors [4 - 10].

-	Si	Ge	GaAs	4H-SiC	InN	AlN	GaN
Energy Bandgap (eV)	1.1	0.66	1.42	3.25	0.7	6.2	3.39
Direct (D) /Indirect (I)	I	I	D	I	D	D	D
Electron Mobility ($cm^2/V \cdot s$)	1400	3900	8500	620	1000	700-980	1000; 2000 (2DEG)
Density (g/cm^3)	2.3	5.32	5.3	3.2	6.78	3.26	6.15
Breakdown Field (MV/cm)	0.3	0.1	0.4	2.0	-	11.7	3.3
Thermal Conductivity ($W/m \cdot K$)	130	58	55	700	450	285	110
Elastic Modulus (GPa)	165	122	118	605	224	390	398

Another type of GaN sensing device is based on nanostructures such as particles, tubes, wires, *etc*., and coating of rare metals (usually Pt) as sensing interfaces, as depicted in Fig. (**1b**) [11 - 13]. During sensing operations, the nano-patterned GaN elements or rare metals can highly respond to the sensed substances, thereby modifying the properties of the device, such as barrier height, depletion region depth, and charge-carrier recombination.

In addition to the aforementioned schemes, optical sensing based on GaN-based integrated devices has received increasing interest due to their excellent properties, such as widely tunable direct bandgap, high efficiency, high stability, *etc* [14, 15]. For instance, the internal quantum efficiency above 90% on GaN-based LEDs is achieved according to recent reports, and the lifetime of GaN-based LEDs is estimated to be 1000-6000 hours when biased at 20-70 mA at 23-85 °C [16 - 18]. Reliability and stability tests are also widely explored by placing the GaN-based LEDs under conditions of moisture, electrical, temperature, *etc.* In particular, on-chip integration is a viable approach for developing a compact sensing system by assembling a light source, photodetector, and sensing interface on a single platform, as shown in Fig. (**1c**) [19, 20].

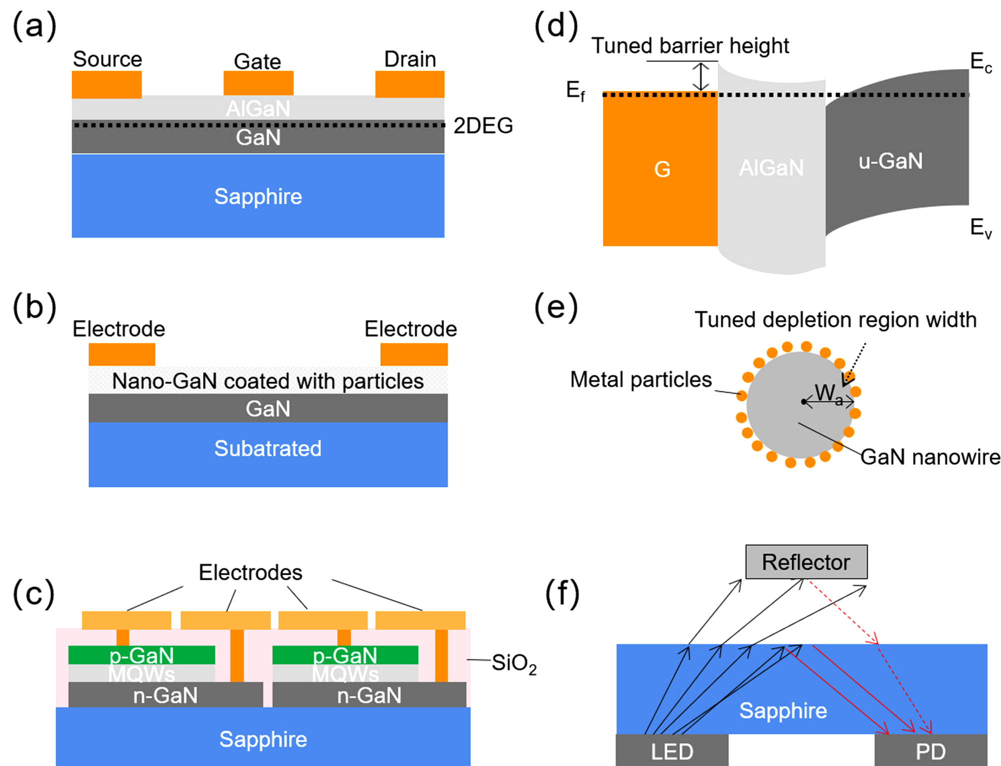

Fig. (1). Schematic illustration of (**a**) typical HEMT-based GaN sensor, (**b**) nanostructured GaN sensor and (**c**) optical GaN sensor. (**d-f**) Corresponding sensing principles.

In this chapter, a detailed discussion of GaN-based integrated optical devices for sensing is divided into five sections. Section 1 introduces the GaN sensors along with an overview of their sensing principles. Section 2 focuses on the GaN-based integrated optical devices and analyzes their sensing mechanisms. Sections 3 and 4 highlight the working of optical sensors operating in reflection and refraction modes. Section 5 concludes with a discussion and a brief summary.

SENSING MECHANISMS OF GAN-BASED INTEGRATED OPTICAL DEVICES

For the GaN-based integrated optical devices, the on-chip components play an important role in determining their sensing performance. Using wafer-scale microfabrication processes, a light-emitting diode (LED) along with a photodetector (PD) as a core component is formed with an epitaxial structure consisting of an undoped GaN layer, n-GaN layer, an InGaN/GaN multiple quantum well (MQW), and a p-GaN layer, as shown in Figs. (**2a** and **b**) shows the

CHAPTER 3

Phosphor-Converted III-Nitride Nanowire White Light-Emitting Diodes

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Abstract: III-nitride nanowire light-emitting diodes (LEDs) have emerged as the next-generation solid-state lighting technology. Currently, white-light LEDs rely on the phosphor-converted white LED (pc-WLEDs) technology, which normally depends on the mixture of blue/ultraviolet emitters and green/yellow/red color-converters. In this chapter, a summary of current research progress on nanophosphors and their applications in improving the device performance of InGaN nanowire pc-WLEDs in terms of color rendering properties and optical and electrical characteristics is presented. These investigations have concentrated on manufacturing methods, morphologies, optoelectronic characterizations and device performances. By concentrating on these critical elements, our goal is to contribute valuable insights and advancements to the field, paving the way for the continued development and application of III-nitride nanowire LEDs in the landscape of solid-state lighting technologies.

Keywords: Blue/ultraviolet emitters, III-nitride nanowire, InGaN nanowire pc-WLEDs, Nanophosphors, Phosphor converted white LED (pc-WLEDs), Solid-state lighting technology.

INTRODUCTION

GaN-based light-emitting diodes (LEDs) have been identified as a promising future lighting technology for solid-state lighting. Moreover, nanostructured LEDs provide several key features that are ideal for wearable microdisplays, augmented reality (AR) and virtual reality (VR) headsets, disinfection, and medical applications [1 - 3]. Nanowire or nanorod LEDs have been demonstrated either by top-down or bottom-up approaches, which show superior performance

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compared to their conventional quantum well counterparts [4 - 6]. Additionally, micro-LEDs utilizing nanowire structures have been realized for full-color displays [7 - 9]. Phosphor-free white LEDs in micrometer scale (μWLEDs) have been intensively studied and reported [10 - 16]. Nonetheless, the low efficiency and efficiency droop are the major limiting factors of deep green to red nitride-based LEDs. The suitable and strong light-emitting materials for high-brightness blue LEDs have been studied to supplement blue emission, providing an optimum white light. Luminescent materials combined with blue LED chips are referred to as phosphor-converted white LEDs (pc-WLEDs). Recently, a hybrid structure of InGaN nanowire LED and yellow- or red-emitting nanomaterials has been studied for high-efficiency white-light emitters [17 - 21]. In this context, current achievements in the device fabrication techniques and structural and optoelectronic properties of these types of WLEDs are presented.

Luminescence Nanomaterials

Luminescence materials or phosphor converters are made up of an inorganic substance (the host lattice) and an activator (which is spread throughout the host crystal in minute proportions). The quantum dots (QDs) are heterostructure semiconductors with particle sizes in the range of 1 to 10 nm, which have a few hundreds to thousands of atoms. The electromagnetic spectrum of both the emission and absorption of QDs can be varied over a relatively large wavelength range by controlling their sizes and compositions, thus enabling diverse color emissions. The first quantum dots generation is cadmium-based quantum dots. In the past decades, they attracted much attention because of their broad ultraviolet (UV) excitation, narrow emission, high quantum yields (QY), bright photoluminescence (PL), and are applied in many fields, such as bioimaging, thermos-electronics, photovoltaic devices [22, 23]. This feature, combined with a large extinction coefficient, high PL QY, narrow-band emission and low light scattering, makes QDs ideal phosphors for WLEDs with high luminous efficacy of radiation (LER) and high color rendering properties. In addition, the narrow-band emission of QDs may provide better color saturation and a larger color triangle, which are highly desired for display backlight applications. However, the presence of cadmium is harmful to human health and the environment. Zinc selenide, the second quantum dots generation that is emitted in the blue-violet region, has a bulk band gap and a bulk Bohr exciton radius of ~2.7 eV and ~4.5 nm, respectively [24]. The ZnSe QDs, whose luminescence and absorption can be turned in a broad band of UV to visible light by impurities doping, are remarkably applied in photocatalysts, LEDs, solar cells, and sensors. The ZnSe QDs synthesis is simple, reproducible and less expensive because of the high solubility and low reactivity of Zinc precursors [24 - 26]. However, the low quantum efficiency of ZnSe QDs limited their applications in industry.

Currently, metal halide perovskites are expected to promising candidates for applications in optoelectronic devices. The halide perovskite general formula is ABX_3 where A is an inorganic/organic cation such as $CH_3NH_3^+$, $CH(NH)_2^+$, Cs^+, B is a metal ion such as Pb^{2+}, Sn^{2+}, Bi^{2+} and X^- is a halide anion or halide mixture of Cl^-, Br^-, I^- [27 - 29]. A-cations with larger radii occupy the corner positions. B-cations with smaller radii are located at the center positions. Halide anions (X^-) are centered on planes of the unit cell. Perovskites exhibit high photoluminescence quantum yield (PLQY) with adjustable bandgap energies, narrow emission, and strong charge-carrier mobility. Their emission color can be easily turned from UV to near–infrared wavelengths by changing the composition or amount of halide anions, as shown in Fig. (**1**).

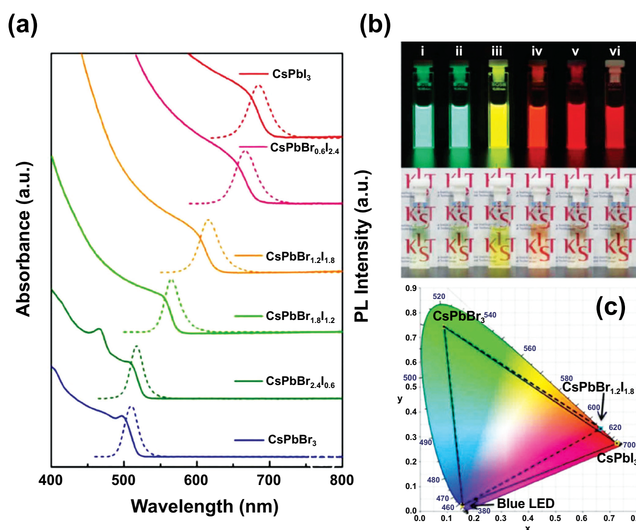

Fig. (1). (**a**) Absorption and emission spectra of $CsPbBr_{3-z}I_z$ PQDs; (**b**) picture of $CsPbBr_{3-z}I_z$ PQD solutions under UV light (top) and indoor light (bottom) [i: z = 0, ii: z = 0.6, iii: z = 1.2, iv: z = 1.8, v: z = 2.4, and vi: z = 3.0]. (**c**) CIE diagram of blue LEDs, $CsPbBr_3$, $CsPbBr_{1.2}I_{1.8}$, and $CsPbI_3$ [29].

Cesium lead halide perovskite (CLHP) QDs were synthesized *via* colloidal and emulsion methods at a high temperature of 120–220 °C using alkyl-amines and fatty acids as ligand shell; the quantum yield of prepared QDs was 40-83% [30, 31]. Particularly, the morphology developments of CLHP perovskite nanoparticles depended on the chain of fatty ligands and temperature. The nucleation and growth mechanism of CLHP QDs takes place at a very fast time scale of milliseconds to several seconds [32]. A recent evolution for the preparation of highly crystalline perovskite QDs is a room-temperature precipitation technique assisted by polar solvents. Interestingly, 95-100% PLQY was achieved for the green/red emitting monoclinic $CsPb(Br/I)_3$ QDs [33]. Despite the numerous advances reported, the biggest obstacle of perovskites is

CHAPTER 4

Effect of Non-Square Potential Profile on Electron Transport Lifetime in $Al_xGa_{1-x}As$-Based Double Quantum Well Structures

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Abstract: The electron transport lifetime τ in low-dimensional semiconductor devices based on quantum well structures is an important parameter that decides the transport as well as optical properties. In recent times, the utilization of non-square quantum well structures has boosted the optoelectronic device performance. This chapter reports the variation of τ with the applied electric field F_{app} in $Al_xGa_{1-x}As$-based modulation doped double quantum well (DQW) structures by considering non-square potential profiles such as parabolic (P), V-shaped (V), semi-parabolic (SP), and semi-V-shaped (SV). Here, τ is analyzed by adopting ionized impurity (imp) and alloy disorder (al) scatterings. In the case of DPQW and DVQW systems, two subbands are occupied from $F_{app} = 0$ up to $|F_{app}| = 5.6$ kV/cm. After that, only one subband is occupied. On the other hand, in the case of DSPQW and DSVQW, there occurs the occupation of only a single lowest subband energy level for all F_{app}. It is significant to note that the effect of the scattering mechanism on the subband transport lifetime differs by changing the structure potential. For example, when both lower and upper subbands are filled, in the case of DPQW, the imp-scattering decides τ, whereas, in the case of DVQW, both imp- and al-scatterings equally contribute. The results of τ in the structures given below are compared with the conventional double square quantum well (DSQW) structure and show that τ (DPQW) > τ (DVQW) > τ (DSQW) at $F_{app} = 0$. The results of τ in non-square DQW structures will be very helpful in understanding the intricacies of the electro-optical properties of emerging low-dimensional semiconductor devices.

Keywords: Double quantum well structure, Non-square quantum well structures, Transport lifetime.

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INTRODUCTION

Devices based on semiconductors are inevitable in every aspect of modern life. The computer and communication industries rely heavily on the use and development of nano-semiconductor devices in which the physical properties are dominated by quantum effects. As a result, the conventional device geometry transforms from bulk tothe lower dimension [1, 2]. The fabrication of semiconductor nanostructures hinges upon the improvement of epitaxial growth techniques, for example, MBE, MOCVD, *etc.* These techniques facilitate the growth of high-quality semiconductor heterostructures (viz. GaAs/AlGaAs) under precisely controlled conditions, where the electronic behavior essentially becomes two-dimensional (2D) in nature [3 - 6]. The electrons are bound to a thin strip along the growth direction but unbound to move along the interface plane, thus constituting the 2DEG, which demonstrates the quantum size effect [7 - 9]. Due to the advancement of the modulation doping technique, the carriers are intentionally set apart from the ionized donors and confined near the interface plane. Modulation-doped field effect transistors (MODFETs) have been developed, which exhibit high electron mobility μ of 2DEG, enabling high-speed devices [5]. The quantum wells (QWs) are formed in the narrower band gap material containing electrons and holes confined along the growth direction (say z-axis), while their motion in the interface plane, the x-y plane, is free. This causes the quantization of carrier energy alongside the z-axis, *i.e.*, perpendicular to the interface plane exhibiting discrete energy levels. This quantum size effect has been utilized to understand the electronic structure properties of materials. By applying electric and magnetic fields, it is possible to control and observe the quantum mechanical effects of the 2DEG, which leads to novel phenomena of mobility modulation, resonant tunneling, integral and fractional quantum Hall effects, resistance resonance, *etc* [7, 10 - 12].

The MBE not only helps to grow the two-dimensional GaAs/AlGaAs QW system precisely but also makes it possible to realize the desired shape of non-square QW potential structures [3, 13 - 15]. The structural change in the configuration of the QW systems, either square or non-square quantum wells (NSQWs), manipulates the carrier confinement. This leads to modulating properties, such as transport and optical nature of novel optoelectronic devices [16 - 19]. The NSQW structures have been developed by altering the band edges of a graded $Al_xGa_{1-x}As$ alloy semiconductor through the appropriate variation of the alloy fraction x within the structure. The carrier transport in different NSQWs also yields notable results [20 - 25].

Although a double quantum well (DQW) is a simple system, it reveals the unique effect of tunnel coupling [26, 27]. The discrete subband energy levels and

eigenfunctions of each well interact weakly through the intermediate barrier, exhibiting coupling that has a substantial influence on the optoelectronic properties of the quantum well systems [26]. Several efforts have also been made to relate the coupling of subband states to the carrier transport properties in different QW structures [28, 29].

Ever since the advent of modulation doping, persistent efforts have been made in the study of carrier transport in semiconductor QW systems [13, 29 - 31]. The introduction of an electric field F_{app}, which is orthogonal to the interface plane of a modulation-doped QW, revises the potential profile of the system, leading to a change in the subband energies E_i, wave functions Ψ_i, and 2D- electron density n_i [6, 7, 26]. The field-induced transfer of subband electronic states also significantly affects the subband electronic properties, such as optical transition and carrier transport in QW-based nanoelectronic devices [32 - 35].

This chapter reports the impact of electric field F_{app} on low-temperature multisubband electron transport lifetime τ in barrier delta-doped DQW structures. The lifetime relates to the electron mobility μ of the system. We consider different non-square DQW systems based on $Al_xGa_{1-x}As$ like Parabolic (DPQW), V-shaped (DVQW), Semi-Parabolic (DSPQW), and Semi-V-shaped (DSVQW). The outside barriers of the above structures are δ-doped symmetrically, and their effects on τ as a function of F_{app} are analyzed.

Here, τ is obtained as a function of F_{app} in $Al_xGa_{1-x}As$-based modulation-doped DQW with different non-square potential structures. We consider the occupancy up to two subbands and calculate τ by involving ionized impurity (imp-) and alloy disorder (al-) scatterings. It is shown that, for DPQW and DVQW structures, two subbands are occupied at $F_{app} = 0$, and the double subband occupancy continues up to $|F_{app}| = 5.6$ kV/cm. However, for DSPQW and DSVQW, the energy levels vary differently, resulting in the occupation of only the lowest energy for all F_{app}. Different non-square structure potentials influence the scattering mechanisms differently via intersubband effects. For example, for DPQW, the imp-scattering decides τ during the occupation of the double subband; however, for DVQW, both imp- and al-scatterings have equal contributions. We also compare the results of the above non-square DQW structures with the conventional double square quantum well (DSQW) structure and show that τ (DPQW) > τ (DVQW) > τ (DSQW) at $F_{app} = 0$. The results of τ in different DQW structures will be very helpful in enhancing the electro-optical properties of emerging low-dimensional nanoelectronic devices.

CHAPTER 5

A Comprehensive Study on High Electron Mobility Transistors

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Abstract: High electron mobility transistors (HEMTs) and III-V compound materials are the key research and development fields for developing improved high-power solid-state devices and integrated circuits (ICs). GaN-based HEMTs have recently gained popularity owing to their usage in high-power and high-frequency applications. This chapter explains different types of heterostructures, principle operations, and basic structures in detail, along with different types of HEMT structures. In order to understand the operation and behavior of the High Electron Mobility Transistor (HEMT) device, internal operation with in-depth analysis is very essential. Therefore, the physics behind the operation of HEMT with proper analysis with the help of neat illustrations is also discussed. Finally, the chapter concludes with a thorough analysis of the breakthrough HEMT architecture and the difficulties posed by HEMTs.

Keywords: Heterojunction, HEMT, Polarization, III-Nitride, 2DEG.

INTRODUCTION

Nitride semiconductors are a special type of material made up of compounds such as Gallium Nitride (GaN), Aluminium Nitride (AIN), Indium Nitride (InN), and their alloys. Nitrides encompass a substantially wider variety of bandgaps as compared to the majority of other materials [1, 2]. Significant developments in wide bandgap semiconductor technology and the utilization of group-III nitrides have rendered the possibility of the development of AlGaN/GaN HEMTs [3, 4]. A field-effect transistor that uses a junction between two different materials with differing band gaps as a channel rather than a doped region is referred to as an HEMT (High electron mobility transistor), also known as a heterostructure FET (HFET) or a modulation-doped FET (MODFET) [5]. The heterostructure HEMT was developed by Dr. Takashi Mimura at Fujitsu Laboratories Ltd. In Kawasaki,

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Japan, in the early 1980s, it was the result of extensive research on III-V compound semiconductor high-frequency and high-speed devices. The first HEMT was developed using the AlGaAs/GaAs material system. Ray Dingle and his colleagues at Bell Labs initially demonstrated the principle idea of modulation doping in 1978, and it is the concept that underlies how HEMT functions today [6, 7]. The high-speed switching properties of HEMT devices emerged from the early device development in 1981 when Fujitsu exhibited a ring oscillator switching at a delay of 17.1 ps [1]. In the first HEMT, integrated circuit, enhancement and depletion mode logic were both used. HEMTs have become crucial parts of the devices with the lowest noise features as a result of more stable technology and advancements in manufacturing processes [8]. GaAs MESFETs were replaced with HEMTs as a result of the manufacturing process's development, which significantly reduced the size of antennas.

Compound semiconductors in the Group III-V nitride family, including Gallium Nitride (GaN) and aluminum gallium nitride (AlGaN), have an exceptional combination of characteristics, including a significant breakdown field, a wide energy band gap, excellent thermal conductivity, outstanding mobility, and a substantial saturation velocity. GaN-based devices perform better for power electronic applications than conventional Si- and SiC-based devices as a result of these characteristics [9].

Early in the 1990s, heterojunctions based on nitride semiconductor AlGaN/GaN HEMT were implemented for the first time. The most widely recognized material systems in which HEMTs have been produced are the AlGaAs/GaAs and AlGaN/GaN structures [10, 11]. An interesting monograph on HEMT development, in the words of Dr. Mimura, is available in the literature [12]. HEMT is widely used today in devices such as cryogenic low noise amplifiers, radio telescopes used to detect microwave signals from dark nebula transmitting satellite receivers, mobile phone handsets, and vehicle radars.

AlGaN/GaN HEMT has the unique ability to generate 2DEG without the use of any extra doping techniques. This distinctive characteristic is primarily a result of the spontaneous polarization and piezoelectric properties that developed in III-nitrides. GaN-based HEMTs have significant benefits over competing technologies compared to other materials' characteristics [13]. More specifically, when compared with other materials with similar output power, GaN's high output power density enables the production of devices that are substantially smaller in size.

BASIC STRUCTURE OF HEMT

The structural cross-sectional view of a basic HEMT is illustrated in Fig. (**1**). The heart of the HEMT is the development of two-dimensional electron gas (2DEG) in a triangular-shaped quantum well. The 2DEG is developed by appropriately choosing the material system. In a HEMT, the barrier layer is a wide bandgap material, and the buffer layer constitutes a narrow bandgap material. The barrier layer and buffer layer may have the same doping type, n-type, forming a heterojunction. Generally, the barrier layer doping is greater than the buffer layer doping. Electrons diffuse when they come into contact, from the wide bandgap barrier layer to the narrow bandgap buffer layer, to produce the lowest energy configuration. This electron transfer continues until a built-in electric field balances out the diffusion, which is akin to how a PN junction operates. Thus, the Fermi level on both sides gets aligned inside the structure, and the spatial change of the Fermi level across the junction is zero. The conduction band and valence band bend appropriately under the equilibrium state. Band bending in the channel region fosters the development of a two-dimensional quantum well that has a finite energy barrier height and width. The electrons are confined to quantized energy levels because of a quantum mechanical mechanism. The charged particles in the channel are restricted to the quantum well and stay at appropriate energy levels, producing a 2DEG [14].

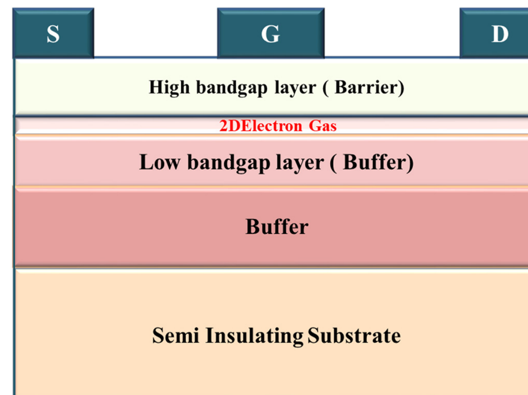

Fig. (1). Basic cross-sectional view of HEMT structure.

The n-doped barrier layer supplies electrons that keep the charge carriers (electrons) in the channel spatially apart from their ionized donor atoms and reduce scattering of mobile charges by impurities. Additionally, the surface scattering is decreased since the current carrying zone is far from the surface. Due to the fact that both occurrences mentioned above enhance carrier mobility, these transistors are called high electron mobility transistors. The carrier mobility is

CHAPTER 6

Study of DC Characteristics of AlGaN/GaN HEMT and its Compact Models

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Abstract: In this chapter, studies of the DC characteristics of AlGaN/GaN HEMT (High Electron Mobility Transistor) and its compact model are presented. It includes the working principles of different HEMT models, their advantages, and their use in high-frequency and high-power applications. The chapter provides a distinct idea about the properties of different models (EE, ASM, and MVGS) and their DC characteristics, which are generated by the Advanced Design System (ADS). The performance analysis of the proposed HEMT models in terms of high electron mobility, high-power and high-frequency operation, low noise amplification, and high thermal stability, along with challenges and future scopes, is discussed in this chapter.

Keywords: ASM, EE, HEMT, Polarization, MVGS3e, 2DEG.

INTRODUCTION

The high electron mobility transistor (HEMT) is a semiconductor device that has gained significant attention in the field of electronics due to its exceptional high-frequency performance and high-power handling capability [1 - 4]. HEMTs are based on a unique transistor structure and utilize specific materials to achieve their superior characteristics. HEMTs are typically fabricated using compound semiconductor materials, such as Gallium Nitride (GaN), Indium Phosphide (InP) or Gallium Arsenide (GaAs) [5]. These materials have a wide bandgap, which allows HEMTs to operate at higher voltages and temperatures compared to other semiconductor technologies like silicon [6].

The foundation of HEMTs lies in their heterostructure design, which consists of different semiconductor layers with varying energy band gaps. This design develops a two-dimensional electron gas (2DEG) channel at the interface between

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layers. The 2DEG channel in HEMTs exhibits high electron mobility, enabling fast electron movement and excellent high-frequency performance [7 - 9].

HEMT offers several advantages over other transistor technologies. It provides high electron mobility, allowing for fast switching speeds and efficient high-frequency operation. Additionally, HEMTs have low power consumption, making them suitable for portable and battery-operated devices [10].

HEMTs, with their unique heterostructure design and compound semiconductor materials, offer exceptionally high-frequency performance, low noise characteristics, and high-power handling capabilities. These attributes make HEMTs a compelling choice for applications where high-speed, high-frequency operation and power amplification are crucial [11].

Motivation toward HEMT

Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are key components in digital logic circuits, power amplifiers, switching circuits, and many other applications. It consists of four terminals: Gate (G), Source (S), Drain (D), and Bulk (B). It is a planar device fabricated on a substrate, typically made of silicon. The channel region connects the source and drain terminals, and it can conduct or block the current flow depending on the voltage applied at the gate terminal [12]. It operates in three modes of operation such as cut-off, triode (linear), and saturation, as depicted in Fig. (**1**).

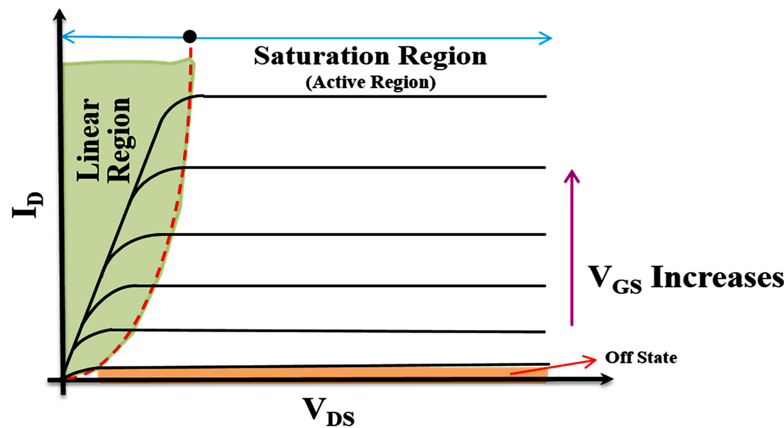

Fig. (1). I-V characteristics of MOSFET.

Cut-off (Off State)

When the gate voltage (V_{GS}) is below the threshold voltage (V_{Th}), the MOSFET is in the cut-off region and no current flows between the drain and source terminals.

Linear Region (Triode Region)

When V_{GS} is above V_{Th} but the drain-to-source voltage (V_{DS}) is small, the MOSFET operates in the triode region. In this mode, the MOSFET acts as a variable resistor, and the drain current (I_D) is proportional to V_{GS} - V_{Th} and inversely proportional to V_{DS}.

Saturation Region (Active Region)

When V_{GS} is sufficiently larger than V_{Th} and V_{DS} is large, the MOSFET enters into the saturation region. In the saturation mode, it acts as a current source, and I_D remains relatively constant regardless of V_{DS}.

Similarly, HEMT is a type of MESFET and has four terminals. HEMTs are specialized power semiconductor devices that offer exceptional high-frequency performance and high-power handling capabilities. They are widely used in various applications, especially those requiring high-speed signal amplification and high-power amplification at RF and microwave frequencies [13]. The basics of HEMTs are as follows:

Heterostructure Design

The fundamental feature of HEMT is its heterostructure design, which involves the use of different semiconductor materials with varying energy band gaps. This design creates a two-dimensional electron gas (2DEG) channel at the interface between the layers, as shown in Fig. (**2**).

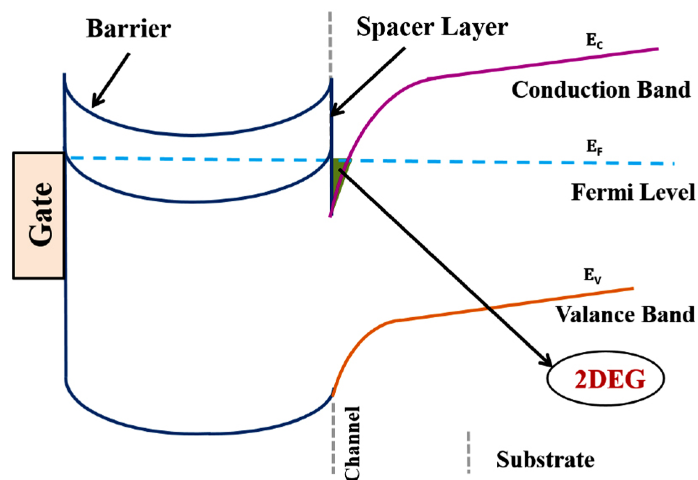

Fig. (2). Generalized energy band diagram of HEMT.

CHAPTER 7

An Overview of Reliability Issues and Challenges Associated with AlGaN/GaN HEMT

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Abstract: GaN-based High Electron Mobility Transistors are currently exhibiting exceptional performance in areas that handle high power, high frequency, *etc.* In particular, their outstanding electrical control characteristics that were demonstrated in HEMT (High Electron Mobility Transistors) based on GaN material made them very promising due to their fundamental and intrinsic unparalleled properties over the existing technologies that use Si-based materials. When a technology enters the manufacturing stage, reliability remains an important challenge. So, it is essential to strongly encourage the knowledge database on the reliability of GaN-based HEMTs. This study focuses on the primary issues that have impacted the reliability of GaN-based HEMTs in both the past and the present. The article focuses on the main problems that have affected the dependability of GaN-based HEMTs both in the past and present, followed by difficulties and potential future applications.

Keywords: 2DEG, Current collapse, GaN, HEMT, Polarization, Power, Reliability, Traps.

INTRODUCTION

The performance of the continuously evolving technological device does not match that of the devices developed with the Si material. These results help in replacing the current technologies with improved and stable innovations that are also expected to demonstrate reliability and efficiency and be more energy-sensitive. As a result, the quest for a novel technology known as HEMT (High electron mobility transistor) is preceded forward by all of these requirements. The HEMT has become the most prominent device for high frequency/high-power and high-speed/high-voltage applications and superior performance and is considered

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the most reliable and cost-effective over traditional Si-based devices [1]. These devices have a unique feature called a Two Dimensional Electron Gas (2DEG), which can be used as a charge carrier in a channel with an excessively large amount. By using heterojunction devices, which have different band gaps between the materials, it is possible to achieve this vital feature.

HEMT was designed with many wide band gap materials in the initial days, but GaN-based HEMT devices are giving remarkable performance over previously developed devices. GaN HEMT devices can offer a reduction in the leakage current at the gate terminal, along with improved drain current and reduced noise. Unlike conventional transistors, HEMT provides improved breakdown voltages using field plate techniques. Nowadays, these high mobility HEMT devices are playing vital roles in many different and distinct applications like 5G communications, the devices of satellite communication that use high power, wireless communication, radars, and guided missiles. Reliability remains a significant problem when a technology moves into the manufacturing stage [2, 3]. So, to ensure the efficacy of GaN technology over other competing technologies, these devices' outstanding performance must be accompanied by excellent device reliability. The knowledge database on the reliability of GaN-based HEMTs is highly recommended.

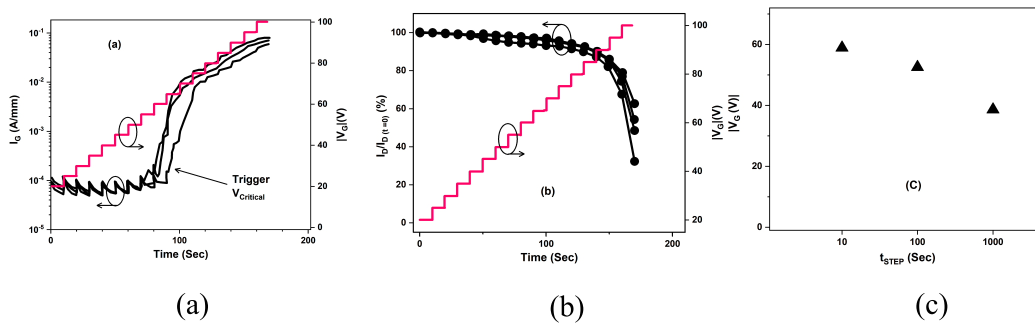
This research examines the primary issues affecting the reliability of GaN-based HEMTs in both the past and present, followed by challenges and future scopes. Finally, the paper concludes with a few final observations on what has been accomplished and what still needs to be done.

RELIABILITY ANALYSIS

Nowadays, studies on the reliability behavior of the GaN HEMT have drastically increased due to the rapid increase of its use in modern technologies. In fact, the exceptional performance of these devices should be overcome by their counterparts with more reliability in terms of success [4]. As per technical papers presented in various reputed journals, the malfunction involved in GaN HEMT diminishes the output current and magnification of leakage current at the gate/drain [5, 6]. These previous research studies showed that the deterioration is mainly due to the inverse piezoelectric effect. The problem occurs due to crystallographic defect formation when the applied voltage is exceeded beyond its given critical value. Consequently, the strain in the AlGaN barrier is increased, leading to an inverse piezoelectric effect [7]. This incidence takes place when the electric field is increased at the gate edge, as also shown by TEM [8]. So, the reduction in the piezoelectric effect not only leads to the failure in holding the current at the output, but also affects the leakage current through the AlGaN

barrier, which turns to an abrupt high spike in the leakage current at the gate terminal [9]. Therefore, further increasing the voltage beyond the critical value will result in the unwanted phenomena of gate leakage and output drain current. In a study, the shortcomings in view of Weibull distribution were explained, introducing a new kind of degradation model that relies on the principles of the percolation track [10].

Some observations recorded by the experimental setup are mentioned in the previous study. In Fig. (**1a**), it can be observed that the gate leakage current is increased with changing step stress but not according to the diminishing current at the output side, which is observed in Fig. (**1b**). Moreover, in Fig. (**1c**), it is clear that the critical voltage entirely relies on the t_{STEP}. Hence, we can say the gate leakage current depends on the time and acceleration of the electric field. In addition to causing substantial current leakage, reverse bias stress also causes a parasitic leakage route path to occur inevitably around the width of the device [11]. If this leakage path is highly distributed, it will definitely have serious and dreadful effects. According to a study, one more cause of degradation is the development of percolation path transition in the AlGaN Layer, which also gives high leakage current [10]. The drop in the output current is because of AlGaN relaxation, which is related to the increased temperature values and lofty electric field. Furthermore, a vital role is played by the quality of interface with the AlGaN barrier, resulting in decreasing current output.



(a) (b) (c)

Fig. (1). a) leakage at the gate during stress, **b**) drop in output current, and **c**) avg critical value based on t_{STEP}.

Most importantly, an infinite loss of current at the output is also being tended to by the higher Al material ratio in the AlGaN proportion. The main factor contributing to the formation of faults in crystallography is the high concentration of Al. So, these two main unwanted phenomena are not related and are completely dependent on other factors [10].

In their study, S. C. Binari *et al.* stated that GaN is highly attractive due to its wide bandgap, concoction element defects, and dopants having a great depth of

CHAPTER 8

Next Generation High-Power Material Ga_2O_3: Its Properties, Applications, and Challenges

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Abstract: Gallium Oxide (Ga_2O_3) is an emerging semiconductor material that has gained significant attention in the field of electronics due to its unique properties and potential applications. Gallium Oxide has a very large bandgap of around 4.8-4.9 eV; this wide bandgap allows gallium oxide to withstand higher breakdown voltages and is well-suited for high-power switches, high-voltage rectifiers and inverters. Gallium oxide-based power electronics can operate at higher voltages and temperatures, enabling efficient energy conversion and reducing losses. In this book, we have discussed the physical properties, growth, and deposition methods along with the various applications of Gallium Oxide. We have even simulated a Gallium Oxide FINFET and discussed its electrical parameter's behavior and various RFIC parameters for different fin widths.

Keywords: FINFET, Gallium oxide (Ga_2O_3), RFIC.

INTRODUCTION

Gallium oxide Ga_2O_3 is a member of the TSO (transparent semiconducting oxides) family of conducting oxides. Despite being well-known for many years, gallium oxide was only occasionally included in mainstream research. Gallium oxide has a long history, going back to 1875 when the newly discovered element gallium and its compounds were first characterized by Lecoq de Boisbaudran [1]. Gallium oxide's traditional applications have never placed a premium on purity and crystalline clarity [2]. However, semiconductor applications have significantly higher requirements for the material's quality and purity, just like those that are recognized for well-known semiconductors like Si or GaAs. Ga_2O_3 research underwent a paradigm shift at this time as the application of the material

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to semiconductors gained new opportunities, and the research community experienced growth.

PHYSICAL PROPERTIES

Polymorphism

The polymorphs of allium oxide that can form are α, β, δ, ε and γ[3, 4]. A transitory K-Ga_2O_3 polymorph is additionally described in another study [5]. In addition to the crystal space group, polymorphs differ within the amount of Gallium ions that coordinate with them. Gallium oxide can be produced in all these phases under certain circumstances [6, 7]. The initial polymorph, α-Ga_2O_3, is rhombohedral, belonging to the R3c space group, and is comparable to corundum (α- Al_2O_3). GaO (OH) can be heated in air between 450 and 550 C to create this polymorph [8]. The second form, β-Ga_2O_3, is monoclinic and belongs to the C2/m space group. Any other polymorph of Ga_2O_3 can be baked in the air at a high enough temperature to produce this version of the material. Little information on other polymorphs is known as a result of their characteristic weak crystallinity making structural characterisation difficult. The third form, γ-Ga_2O_3, is generally acknowledged to have a faulty cubic spinel-type structure ($MgAl_2O_4$-type) with an Fd3 m space group. δ-Ga_2O_3 and ε-Ga_2O_3 were the fourth and fifth polymorphs, respectively, that Roy *et al*. originally synthesized and characterized in 1952 [9]. According to the authors, Mn2O3 and In2O3's C-type rare-earth structures are equivalent to that of -δ-Ga_2O_3 form. In terms of the ε-Ga_2O_3 polymorph, a powder diffraction of the X-ray pattern was measured, which was unique from the remaining known polymorphs even though we were unable to ascertain the ε-polymorph's structure.

β-Ga_2O_3 Properties

The most prevalent and extensively researched polymorph of gallium oxide is the β-form. All other polymorphs are metastable and change into the β- Ga_2O_3 at temperatures over 750-900 C, whereas Ga_2O_3 is the sole polymorph that is stable across the whole temperature range till the melting point [10]. β-Ga_2O_3's thermal stability makes it possible to use high-temperature methods like crystallization, either from melt or vapor phase epitaxy, to create bulk single crystals and epitaxial films. Among other polymorphs of Ga_2O_3, β-Ga_2O_3 has attracted researchers a lot because of its outstanding properties and availability. Even though β-Ga_2O_3 is better characterized than other Ga_2O_3 polymorphs, published data on its material properties still contains some errors.

Crystal Structure

Kohn *et al*. were the first to describe the polymorph of gallium oxide's lattice characteristics, while Geller determined the structure in the space group C2/m [8, 9]. Piezoelectricity and pyroelectricity tests came back negative, supporting the idea that the space group within the crystal was C2/m. Walton noted the crystals' apparent poorer morphological symmetry than the recognized point group 2/m [10]. The lesser symmetry was assigned to β-Ga_2O_3 by optical and SEM tests as well. β-Ga_2O_3's crystal cell has a pseudo-symmetrical triclinic structure, and P1 must be the actual space group. They proposed that the real space group for the crystal cell of β-Ga_2O_3 should be P1 and that it has a pseudo symmetrical triclinic structure. Ahman *et al*. presented a very recent analysis that is even accurate about the structure of β-Ga_2O_3 crystal [11]. The precision of this investigation was nearly ten times greater than in the earlier efforts, even though the results only slightly deviate from the data of Konh and Geller that were previously published [11, 12]. The consistent extensions and X-ray diffraction symmetry convincingly demonstrated a C-centred monoclinic cell with space group C2/m. The structure of space group P1 could not be improved further. Fig. (**1**) represents the β-Gallium oxide unit cell. It contains two positions of Gallium, one with tetrahedral geometry (Ga (I)) whereas the other one has octahedral geometry (Ga (II)), which are not equivalent from a crystallographic perspective. The oxygen ions are organized in a close-packed, "distorted-cubic" array, so three distinct crystallographic places of the oxygen atoms are designated as O(I), O(II), and O(III), respectively. One oxygen atom is coordinated tetrahedrally, whereas the other two are triangulated.

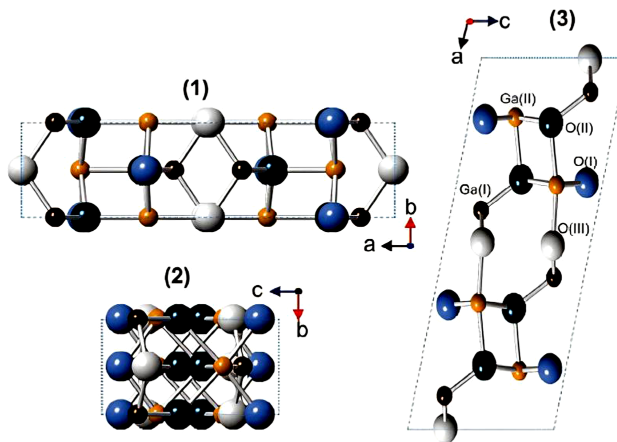

Fig. (1). Representation of β-Ga_2O_3 Unit Cell. Ga_2O_3 possesses two inequivalent Ga sites, Ga(I) and Ga (II), as well as three inequivalent O-sites, O(I), O(II) and O(III) [7].

CHAPTER 9

Investigation of the Impact of Different Dielectrics on the Characteristics of AlN/β-Ga_2O_3 HEMT

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Abstract: In the present research, a β-Ga_2O_3 high electron mobility transistor is proposed for investigating the implementation of high-k dielectric materials. The implementation of the dielectrics, Si_3N_4, Al_2O_3, and HfO_2, at the interface of aluminum nitride (AlN) and the gate is depicted to determine the optimal selection. The novelty of the device lies in the highly doped n+ material with a broader gap between ohmic contact and the barrier layers. The performance is computed regarding the transfer and output characteristics, transconductance, gate capacitance, 2nd and 3rd-order transconductance, sub-threshold voltage, on-resistance and output conductance. The crucial parameters for switching and linearity performance are also assessed. The results demonstrate significant improvements in dynamic and access resistance, leading to a remarkably high transconductance (G_m) value of 0.15 S/µm and a peak drain current density of 650 A/mm at V_{ds} = 5 V. These promising results pave the way for potential applications in high-power radio frequency and microwave devices, making the proposed device a promising candidate for future advancements in these fields.

Keywords: Aluminum nitride (AlN), Buffer layer, Dielectric, Gallium Oxide(Ga_2O_3), HEMT.

INTRODUCTION

The evolving technology is seeking new materials every day, and β-Ga_2O_3 is the evolving material in the technological arena. Researchers have given Ga_2O_3 careful deliberation for a variety of applications, including power devices, Schottky barrier diodes, and photodetectors, because of its wide band gap (4.7 eV), better electron mobility (180cm^2/Vs), higher saturation velocity (2X10^{7}cm/s), and higher breakdown strength (8 MVcm^{-1}). Above all, β-Ga_2O_3 has the ability to be fabricated as a single-crystal substrate, which is phenomenal [1 - 4]. The cherry on the cake for β-Ga_2O_3 is the high Figure-of-Merit (FOM) for photodetectors,

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rendering it more favorable over other materials like Silicon Carbide(SiC) or Gallium Nitride(GaN). These properties collectively contribute to the successful fabrication of modulation-doped double heterostructures, field-effect transistors (FETs), and high electron mobility transistors (HEMTs). A high electric field of 8 MV/cm is observed, which is comparably higher than that of GaN, InAs, and GaAs wide band gap (WBG) semiconductors. The distinguishing factors that set β-Ga_2O_3 apart are its n-type dopants, shallow donors, and adjustable conductivity. The excellent quality of bulk crystals allows for the cultivation of high-quality epilayers using established techniques like czochralski, floating melt growth, and molecular beam epitaxy.

Setting δ-doping position and concentration during fabrication is an intimidating challenge that can be effectively addressed with the support of spontaneous piezoelectric polarization charges. Furthermore, these fabrications have achieved a remarkable ideality factor (1.0) for Ga_2O_3 devices. Also, the research work to date reports that these devices show high reverse breakdown voltage [5 - 8]. To achieve enhanced FETs performance, a promising approach involves the integration of Ga_2O_3 for its high breakdown capabilities with polar III-nitrides (GaN or AlN) known for their strong polarization impact [9].

Likewise, FETs with shorter gate lengths have been created by obtaining low ohmic contact resistances and optimizing channel length. High effective electron mass, maximal carrier mobility at room temperature, and low lattice mismatch are further desirable traits. Ga_2O_3 HEMT surpasses GaN in low-frequency zones, depending on the figure of merit (FOM) and saturation velocity research studies [9 - 12]. The comparison of the figure of merit (FOM) and saturation velocity exhibits the superiority of Ga_2O_3 HEMT over GaN in the low-frequency regions. The device's performance might be adversely affected by heating if the working temperature is higher than 300°C, which can cause a reduction in the performance of significant signals [13]. The β-Ga_2O_3 MOSFETs demonstrate superior performance compared to other parameters, specifically in terms of device heating and scaling [14]. The device's heterostructure may result in a better improvement in terms of the heating effects. Additionally, the device barrier region's delta doping is crucial for creating a 2-DEG (Two-Dimensional Electron Gas) at the interface of $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ when polarization is missing from the device. It is crucial to keep in mind that x can possess a value lower than 0.40 since doping at the interface gets harder as x increases [15 - 17]. Due to their non-polar and stable characteristics, the β-Ga_2O_3 HEMTs exhibit better performance than other devices in terms of transport characteristics, DC output performance, electric field, and breakdown voltage. With increased charge densities, the decrease in cutoff frequency can be explained to some extent by a decline in effective potential. Furthermore, the device's non-polarity permits δ-doping in the barrier area, which

facilitates the induction of a 2-DEG in the channel. The polarization metric, however, has benefits such as greater device performance. The theoretical performance of the devices with β-Ga_2O_3 is achieved by taking advantage of the low defect density of the β-Ga_2O_3 HEMT device. The length of drift area and β-Ga_2O_3's doping density may typically be reached using the existing film growing technique. The higher band gap energy and the presence of small drift regions in β-Ga_2O_3-based devices contribute to pushing the avalanche breakdown to higher electric field values (8.1 MV/cm). However, this scenario poses challenges in terms of field management at the junction interface and along device edges. β-Ga_2O_3 has proven to be a suitable material for designing power devices with breakdown voltage exceeding 100 kV. This research work proposes and simulates the β-Ga_2O_3HEMT for different dielectric materials in Silvaco TCAD [18]. We conducted a comprehensive performance analysis of the AlN/β-Ga_2O_3HEMT device, comparing transfer and output characteristics as well as switching and linearity parameters for all the dielectrics to conclude for the optimum. This analysis was conducted using various dielectrics, specifically Si_3N_4, Al_2O_3, and HfO_2, employed at the interface between AlN and the gate. The major properties and values of materials, AlN and β-Ga_2O_3, used in the device are given in Table **1** [1, 19].

Table 1. Major properties of AlN and β-Ga_2O_3HEMT.

Parameter	Units	AlN [19]	β-Ga_2O_3 [1]
Bandgap	**eV**	**6.1**	**4.9**
Affinity	eV	1.4	3.15
Dielectric Constant	-	8.5	8.2
Electron Effective Mass	m_0	0.33	0.227
Electron Mobility	cm^2/Vs	426	180

In this work, AlN/β-Ga_2O_3 MOSHEMT with high-k dielectric Si_3N_4, Al_2O_3 and HfO_2, used as the passivation layer, is presented. Section I gives a brief overview and the underlying principle for MOSHEMTs. Section II describes the proposed device structure of AlN/β-Ga_2O_3MOSHEMT. Section III discusses the DC analysis and linearity parameters for β-Ga_2O_3 MOSHEMT. The device is designed and analyzed for total gate capacitance, $I_{on/off}$, threshold voltage, and subthreshold swing. To analyze the linearity of a device, transconductance, g_{m2}, g_{m3}, and output conductance of Si_3N_4, Al_2O_3 and HfO_2 are considered. The conclusion and prospects of the work are discussed in Section IV.

CHAPTER 10

InAs Raised Buried Oxide SOI-TFET with N-type $Si_{1-x}Ge_x$ Pocket for Low-Power Applications

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Abstract: In this chapter, we studied the device-level performance based on electrostatic parameters of a source pocket engineered raised buried oxide (RBOX) SOI tunnel field-effect transistor (SP-RBOX-SOITFET). Using $Si_{1-x}Ge_x$ pockets between the channel and the source, steep subthreshold swing transistors can be obtained. In the pocket, a narrow n+ region is formed by a tunneling junction between the p^+ region of the source. In order to reduce subthreshold swing, the tunneling width must be narrowed, and the lateral electric field must be increased. So, the studied structure can be used to design the dielectric modulated biomolecule biosensors for IOTs applications. Simulation analyses of the proposed work has been conducted using the Silvaco ATLAS TCAD tool.

Keywords: DC/RF parameters, Heterojunction, Internet of things (IOTs), SOI TFET, $Si_{1-x}Ge_x$, Source Pocket Engineered.

INTRODUCTION

In the current scenario, electronic equipment are becoming necessary for everyone in every field. We require electronic equipment for children so that they can attend their classes, and teachers require equipment to deliver classes. Therefore, we can imagine how much we depend on electronic equipment. All electronic equipment is made up of ICs. The use of a computer is now slowly replaced by smartphones; people want portable equipment for their work but not at the cost of performance. So, there is a need for technology that reduces the size of ICs and enhances the performance. It was Gordon Moore who predicted in 1965 that every year, transistor count would be double for the same area of the chip, and after a decade, he modified his statement to every two years [1]. To follow Moore's law, there is a need of constant scaling of transistors [2]. The scaling of transistors

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requires the scaling of device's parameters like channel thickness, oxide thickness, threshold voltage, supply voltage, *etc.*, along with the device dimension [3, 4]. MOSFET has certain limitations due to which its scaling has reached saturation. Further reduction in size causes two main problems. Leakage current and difficulty in reducing the supply voltage [5]. Significantly, the Tunnel FET (TFET) is a popular alternative device among academics these days [6 - 12]. The main objective of TFET is to achieve a high value of ON-current (I_{ON}) and the lowest value of average subthreshold swing S_{avg} over five decades of drain current [13 - 15]. Also, the OFF-state current (I_{OFF}) has to be kept as low as possible. The target values for such requirements are I_{ON} as high as 100 milliamperes, S_{avg} below the MOSFET limit of 60 mV/decade and a high ON by OFF current ratio in the order of 10^5 at a drain voltage of 0.5 volts. In order to have a high value of ON-current, the tunneling probability should be as high as possible and become close to unity for small values of gate voltage. So, the higher the tunneling probability value, the more the electrons, giving rise to high I_{ON} [16 - 17]. InAs is a compound semiconductor composed of indium and arsenic. It has desirable electronic properties, particularly for high-speed and low-power applications. InAs has a narrow bandgap, which can be advantageous for TFETs as it allows for efficient quantum tunneling. InAs TFET refers to a Tunnel Field-Effect Transistor where the semiconductor material used for the transistor is Indium Arsenide [18]. Such devices are of interest in the field of advanced semiconductor technology, particularly for applications where low power consumption is critical, such as in portable devices and energy-efficient electronics [18, 19]. The use of InAs as the semiconductor material helps exploit its specific electronic properties for efficient tunneling through the transistor barrier [20]. InAs SOI TFET represents a tunnel field-effect transistor where the active semiconductor material is Indium Arsenide (InAs), and the device is fabricated using Silicon-On-Insulator technology [21]. This combination aims to leverage the desirable electronic properties of InAs for tunneling while benefiting from the advantages of SOI technology in terms of reduced power consumption and improved transistor performance. Such advanced transistor technologies are explored for applications in low-power electronics and high-speed devices [22]. A Silicon-Germanium (SiGe) pocket Tunnel Field-Effect Transistor (TFET) is an interesting device in the field of analog and radio-frequency (RF) circuit design [23]. TFETs are potential candidates for low-power applications due to their unique tunneling mechanism for charge transport, which allows for steep sub-threshold characteristics and reduced leakage currents. The addition of a SiGe pocket in the TFET structure can enhance its performance further. Here, a brief analysis of the RF/analog characteristics of a SiGe pocket TFET [23 - 25]. Raised buried oxide (RBOX) typically refers to a technology used in the fabrication of Silicon-On-Insulator (SOI) substrates [26]. SOI is a semiconductor substrate where a layer of silicon is separated from the bulk silicon

by a buried oxide (BOX) layer. The BOX layer provides electrical isolation between the silicon layer and the bulk substrate [27].

In this work, with InAs as the source material, $Si_{1-x}Ge_x$ source pocket raised buried oxide (RBOX) SOITFET structures have been studied using electrode of aluminum (work function, Φm=4.08). The RBOX concept is used to minimize leakage currents and improve ON-state currents [28]. A comparison has been made between the performance parameters of our proposed device (SP-RBOX-SOITFET) and the same TFET structure using silicon instead of InAs as the source material. This chapter is divided into four sections: Section 2 presents the device structure and simulation setup, Section 3 presents results and discussion based on the TCAD tool for electrostatic analysis, and Section 4 concludes this work.

METHODOLOGIES FOR SIMULATING DEVICE STRUCTURE

Silvaco TCAD (Technology Computer-Aided Design) is a suite of tools designed for simulating semiconductor processes, devices, and circuits [29]. Simulating device structures using Silvaco TCAD involve several steps. There are many statements involved in DECKBUILD to build a structure. The order in which they are specified is also very important, which is as follows:

Group		Statements
1- Structure specification	----------------------	MESH REGION ELECTRODE DOPING
2- Material Models specification	----------------------	MATERIAL MODELS CONTACT INTERFACE
3- Numerical Method Selection	----------------------	METHOD

CHAPTER 11

SiGe Source-Based Epitaxial Layer-Encapsulated TFET and its Application as a Resistive Load Inverter

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Abstract: In this study, a SiGe source-based epitaxial layer-encapsulated TFET (SiGe source ETLTFET) is developed, and the performance of the device is examined by optimizing various design parameters, including the epitaxial layer thickness (t_{epi}), gate-to-source overlap length (L_{ov}), Ge mole fraction, and source doping concentration. The average subthreshold swing (SS_{avg}) and ON-OFF current ratio are used to evaluate the device's performance. The results show a superior performance of SiGe source ETLTFET compared with its homojunction counterpart. Furthermore, to demonstrate the possibilities for using the proposed device in a logic circuit, a resistive load inverter is designed using the n-type ETLTFET.

Keywords: Epitaxial Layer, Inverter, Line Tunneling, Silicon Germanium, TFET.

INTRODUCTION

Recent years have seen a rise in interest in the Tunnel Field Effect Transistor (TFET) owing to its resilience to short channel effects and sub-KT/q subthreshold swing [1, 2]. Inter-band tunneling conduction process makes the TFET device a potential candidate to surpass the constraints of conventional MOS [1]. Engineering of materials and structural design are being extensively researched to create a modified TFET device that outperforms the traditional MOSFET [3 - 6]. The performance of TFETs was found to be improved by vertical BTBT owing to the larger tunneling junction area [7 - 10]. In synthetic electric field TFETs (SETFETs), epitaxial layer (ETL)-based vertical BTBT is employed, and it has been discovered that the augmented electric field at the ETL improves the ON current [11]. Since the synthetic EF is high toward the side fin in SETFET, the

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vertical BTBT is obviously ineffective. Therefore, employing the ultrathin ETL encircling the fin, ETLTFET is introduced to improve the efficiency of vertical BTBT [12].

SiGe can be employed as the source material because of its smaller bandgap, according to many studies [13 - 15]. It is important to highlight that SiGe can be commercially generated with a Ge mole fraction (x) of 0.5, utilizing contemporary technology [16, 17]. There are both benefits and drawbacks to adding more Ge. At greater Ge content, an improved leakage current also coexists with an enhanced tunneling current [18].

In this study, we have introduced an Epitaxial layer encapsulated Tunnel FET with a SiGe source. The introduction of the SiGe source in the structural design of simple homojunction TFET modifies the BTBT process [19, 20]. Here, we optimize the device design parameters and investigate its circuit performance using a resistive load inverter.

COMPUTATIONAL DETAILS: SETUP AND CALIBRATION

The 3D and 2D views of the SiGe source ETLTFET are displayed in Fig. (**1**). An epitaxial layer is seen encapsulating the fin structure of the device. The device is made of Silicon material except for the source region, which is made of SiGe. An Arsenic concentration of $1x10^{20}$ cm^{-3} is used in the drain region, whereas very light doping of $1x10^{16}$ cm^{-3} is utilized in both the channel region and the epitaxial region. For the device under discussion, both regions serve as a channel. The gate-drain underlap length (L_{und}) of 20 nm is used to reduce the ambipolar current, and gate-source overlap is incorporated in the proposed design to increase the ION [21]. The gate stack has a metal gate with a work function of ϕ_m=4.2 eV (Al) and an equivalent oxide thickness (EOT) of 0.4 nm with HfO_2 (ε=22) as the oxide material [22]. The optimized value of the fin with fin height (H_{fin}) of 40 nm and fin width (W_{fin}) of 10 nm is taken for the considered device.

The incorporation of the SiGe source creates a SiGe/Si heterojunction. The narrower band gap causes the electric field at the tunneling junction to increase, decreasing the width of tunneling and thus raising the probability of tunneling.

Owing to the smaller band gap, the probability of tunneling increases. This is because of the decrease in tunneling width, which enhances the electric field at the tunneling junction. Besides, the encapsulated epitaxial layer around three sides of the fin permits an additional vertical tunneling perpendicular to the gate along with the usual lateral tunneling. The energy band diagram at both the ON state ($V_{GS} = V_{onset}+V_{DS}$) and OFF state ($V_{GS}$=0 V) is presented in Fig. (**2**).

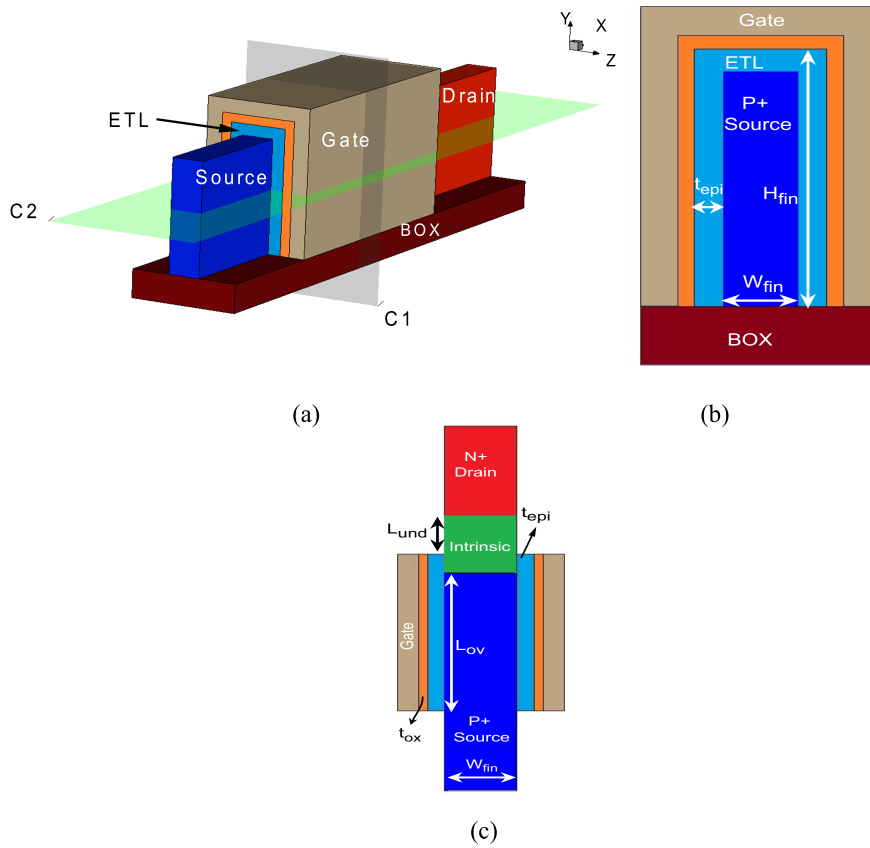

Fig. (1). Schematic view of SiGe source ETLTFET both in 3D and 2D. The 2D view is projected along the cutlines C1 and C2.

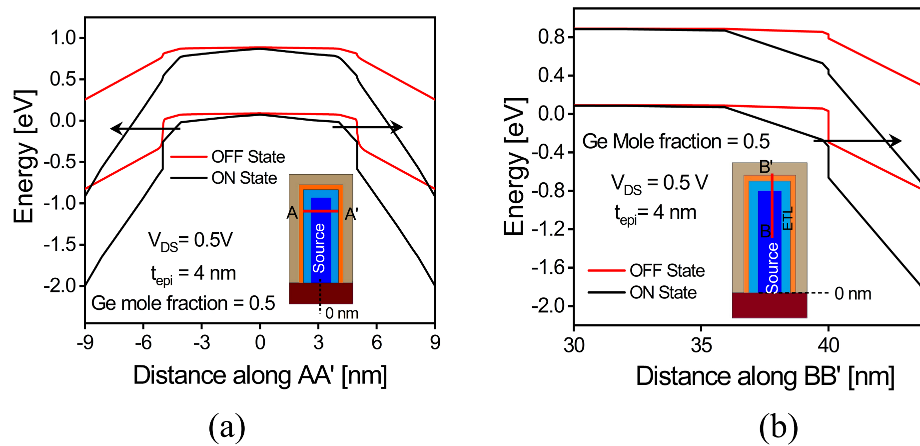

Fig. (2). Energy band diagram showing the banding for SiGe source ETLTFET at both ON and OFF state (**a**) along AA' cutline and (**b**) along BB' cutline of x-plane, as shown in the inset.

CHAPTER 12

Elimination of the Impact of Trap Charges through Heterodielectric BOX in Nanoribbon FET

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Abstract: In this study, a heterodielectric BOX (HDB) Nanoribbon FET (NR-FET) is built using the TCAD device simulator to reduce the effect of trap charges on numerous electrical properties in traditional NR-FETs. Initially, a reasonable study in terms of transfer characteristics of NR-FET is highlighted between homodielectric and HD BOX. Because of the existence of high-k dielectric below the drain area, it is assumed that the impact of trap charges is insignificant in HDB NR-FET. Furthermore, the trap charge effect on transconductance (g_m), total gate capacitance (C_{gg}), and cut-off frequency (f_c) in HDB NR-FETs are investigated. Higher-order harmonics of g_m (g_{m2} and g_{m3}) and linearity parameters are studied for HDB NR-FET in a series of steps. Finally, the effect of temperature on input characteristics, g_m, C_{gg}, f_c, g_{m2}, g_{m3}, and linearity behavior for HDB NR-FET is investigated in the presence of trap charges.

Keywords: BOX thickness, DC parameters, Heterodielectric BOX, Homodielectric NRFET, Linearity performance, Nano ribbon FET, RF/analog parameters, TCAD simulator, Temperature, Trap charge.

INTRODUCTION

An important strategy of the semiconductor industry is the reduction in dimensions of electronic components. According to Moore's law, the number of transistors in an integrated circuit doubles every eighteen months, and the tremendous growth of the electronic industry depends on this law [1]. As highlighted by IRDS, to realize transistors of small dimensions, a large number of limitations and challenges are faced during their manufacturing [2]. Such prominent limitations are short channel effects (SCEs), manufacturing complications, increased power consumption, and increased leakage current, which in turn affect the device performance [3, 4].

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These limitations can be overcome by using vertical channel FET, which is popularly named FinFET technology. Its key advantages are a reduction in SCEs, high transconductance, and reduced leakage current. The channel is wrapped from all sides of the gate, which results in an increased gate area and, thus, improved device performance [5, 6]. However, the performance of FinFET is degraded due to the presence of charge carriers at the corner, which is known as the corner effect. Using gate-all-around (GAA) FETs, where a channel is contributed from all sides of the gate, the corner effect is prevented [7]. The integration of GAA FET using CMOS technology is complicated, and it puts the limitation on GAA FET [8]. To overcome these barriers in FinFET and GAA FET, a new structure known as nanoribbon FET (NR-FET) is reported in the literature [9]. In NR-FET, multiple stacks of nanosheets are placed vertically, which, in turn, enhance the speed without compromising the area [10]. Additionally, the NR-FET fabrication technique is compatible with conventional CMOS technology.

The stack design in NR-FET indicates multiple interfaces of gate dielectric and gate material. The presence of interface trap charges (ITCs) during the radiation process at the Si and gate oxide interface hinders the device's performance. The multiple-gate oxide and gate material interface in NR-FET indicate the existence of a large number of trap charges, which significantly affect the device's characteristics [11, 12]. In the literature, the ITCs' effect on electrical parameters of NR-FET and TFET is reported [13 - 15]. Moreover, researchers have highlighted the effect of ITCs, including environmental temperature, in TFETs [14, 15]. Nowadays, researchers are focusing on graphene-based NR-FET rather than Si technology for high-frequency and biosensing applications [16]. The performance of NR-FET can be further enhanced by utilizing high and low-k gate dielectric near the source and drain regions, respectively [17]. Additionally, when NR-FET ITCs are present, the switching ratio and transconductance generation factor (TGF) deteriorate [13].

The effect of ITC on the device can be minimized using heterodielectric BOX (HDB) instead of homodielectric. In HDB, the high-k HfO_2 is considered near the drain region, whereas low-k SiO_2 is considered for the remaining portion of BOX [18]. Das *et al.* reported that the effect of ITC is nullified using HDB in the FinFET structure [19]. Sahay and Kumar highlighted that ambipolar current can be reduced in TFET through HDB [20]. However, a thorough analysis of the reduction in the influence of ITCs on electrical parameters has not been reported in the literature. In this work, we have described the influence of ITCs on DC, RF/analog, and linearity performance can be minimized using HDB in NR-FET for the variation in BOX height and temperatures.

DEVICE STRUCTURE AND SIMULATION SET-UP

Figs. (**1a** and **b**) show the 3D structures of homodielectric and heterodielectric BOX NR-FETs, respectively. The corresponding 2D schematic of NR-FET is portrayed in Fig. (**1c**). In this case, a stack of three nanoribbons is used to improve device characteristics by enchancing gate control over the channel. SiO_2 is used as the gate dielectric material in all NRs, which are manufactured by Si. For homodielectric, SiO_2 is considered as BOX, whereas, for HDB, the HfO_2 is kept below the drain and SiO_2 for the remaining portion of BOX. A metal with a 4.6 eV work function is regarded as a gate material. The various dimension specifications are summarized in Fig. (**1**). The dimension of each NR is 10 nm×10 nm, the oxide thickness of the gate is 2 nm, BOX thickness and height are 60 and 20 nm, respectively, the gate length is 24 nm, source height is 10 nm, spacing between consecutive source is 6 nm, the height of source/drain is 46 nm.

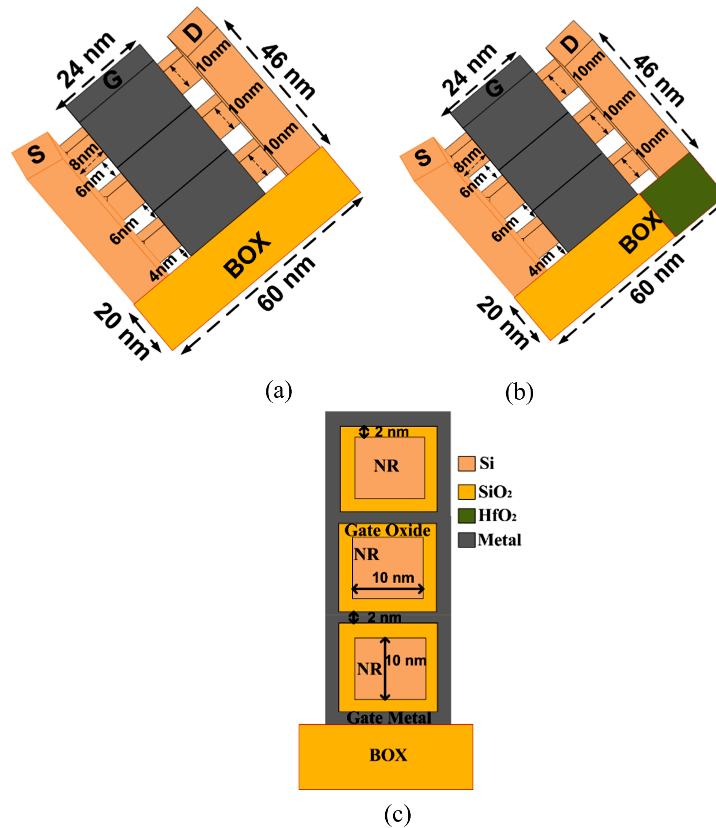

Fig. (1). (**a**) 3D view of homodielectric, (**b**) 3D schematic diagram of heterodielectric, and (**c**) 2D schematic diagram of heterodielectric NR-FETs.

CHAPTER 13

Ge-Channel Nanosheet FinFETs for Nanoscale Mixed Signal Application

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Abstract: Due to the shortening of channel length in accordance with Moore's law, short channel effects degrade transistor performance. This chapter explains the emerging nanosheet fin field effect transistor (FinFET) design and operation through technology computer-aided design (TCAD) tool-based design and simulation. A 10 nm node Ge-channel nanosheet FinFET is designed and simulated by incorporating quantum transport models in both DC and AC environments. Corresponding short channel effect (SCE) parameters are obtained and compared with Si-channel nanosheet FinFETs. Further, device feasibility for low-power and high-frequency applications is studied.

Keywords: FinFET, Ge-channel, High frequency, Low power, Nanosheet.

INTRODUCTION

Owing to aggressive increase in the number of electronic gadgets, the consumers demand Moore's law to be obeyed. This includes scaling down transistors with enhanced performance. However, Moore's law has reached its limit due to adverse short-channel effects in the case of MOSFET [1]. To reduce the same, the device structure is modified to have better gate controllability by increasing the number of gate-to-channel junctions, resulting in the discovery of three-dimensional transistors such as FinFET with a gate wrapped around a thin piece of Si (superiorly undoped), which is also known as "fin", and the current flows along its top and side surfaces [2]. This reduces SCE and leakage current [3]. Another limitation in the downscaling of MOS devices is the depletion region created along the channel at junctions of differently doped semiconductors, which leads to the introduction of junction-less transistors. In these transistors, the

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source, channel, and drain are uniformly doped to avoid any junctions. Junctionless transistors have an advantage over classical MOSFETs due to improved subthreshold slope (SS) and drain-induced barrier lowering (DIBL) required for better analog/RF performance. Recently, many semiconductor companies have succeeded in adopting 10 nm technology while fabricating IC [4]. However, as the gate length is reduced to below 3 nm, the conventional tri-gate FinFET structure is modified to a gate-all-around (GAA) structure in which the gate surrounds the channel from all sides to have better gate controllability. This significantly improves SCE by reducing the operating voltage. GAA-structured transistors can be either nanowire (channel region has a cylindrical and elongated shape) or nanosheet type (channel is in nanosheet shape). Due to less width, the amount of current flowing through the channel is less in nanowire transistors. Whereas, in nanosheet transistors, the area of contact between gate and channel is increased by sheet-like structures [5]. Further, Germanium delivers more mobility than silicon, which is suitable for improved device performance [6]. Hence, in this chapter, the Ge-channel nanosheet FinFET is considered as an example for design, analysis, and study purposes.

In Section 2, the structure of a 10 nm Ge-channel nanosheet FinFET, along with device parameters, is explained. The physical models considered during TCAD simulation are presented in Section 3. In Section 4, the simulation results are demonstrated and discussed. Finally, Section 5 concludes the chapter.

NANOSHEET FINFET STRUCTURE

Nanosheet FinFET structure is a special case of the gate-all-around (GAA) structure, where multiple channels exist between the source and drain. Each channel is surrounded by an oxide layer followed by gate contact in the form of sheets, as shown in Fig. (**1**). The 3D schematic structure demonstrates a nanosheet FinFET with three numbers of channels designed using the Genius 3D Visual TCAD tool offered by Cogenda. The device consists of Germanium (Ge) as the channel material with a gate length (L_g) of 10 nm, Silicon Dioxide (SiO_2) as the source and with a drain side spacer of length 15 nm, Ge for source/drain pad of length 20 nm, and Aluminum (Al) for source and drain contacts of length 1 nm. Device parameters and dimensions necessary during simulation are presented in Table **1**.

Table 1. Various parameters considered during TCAD simulation.

Parameters	Material	Dimensions
Drain/Source contact length	Al	1 nm
Drain/Source Pad Length	Ge	20 nm

(Table 3) cont.....

Parameters	Material	Dimensions
Drain/Source Spacer length	Ge	15 nm
Channel width & length	Ge	10 nm
Gate Width	Poly silicon	24 nm
Drain/Source Spacer Dielectric	SiO_2	
Vertical Fin Pitch	Ge	15 nm
Gate Dielectric Thickness	SiO_2	1 nm
	HfO_2	1 nm
Burried oxide (BOX)	SiO_2	45 nm

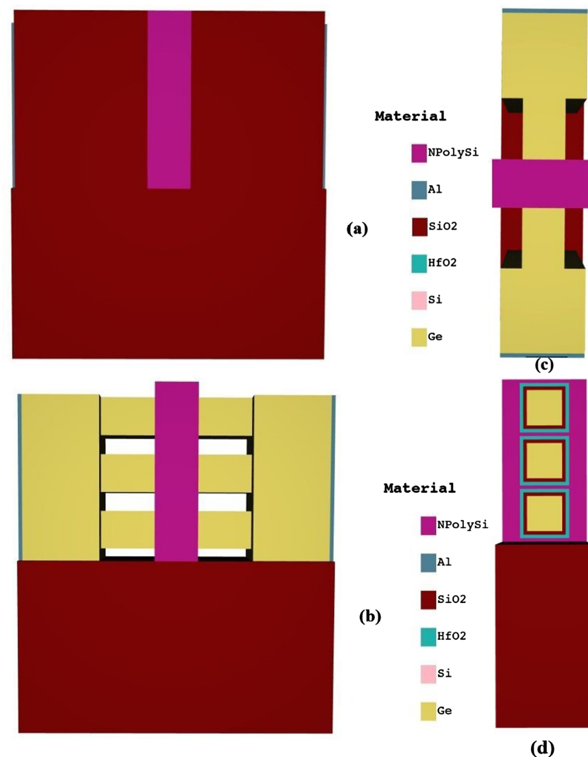

Fig. (1). Schematic views of nanosheet FET from different sides (**a**) front view (**b**) front view without spacer oxide (**c**) top view without spacer oxide (**d**) side view without source/drain and spacer oxide.

DEVICE SIMULATION SETUP

The nanosheet device under study has n-type polysilicon as gate contact with a thickness of 1 nm around the oxide layer, length of 10 nm, and work function of 4.8 eV for obtaining a positive threshold voltage (V_t). The simulation is carried out at a room temperature (300K). The doping concentration of the channel region

CHAPTER 14

Recent Trends in FET and HEMT-Based Biosensors for Medical Diagnosis

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Abstract: Nowadays, a wide range of viruses, bacteria, cancers, and other diseases have emerged due to drastic changes in the environment and climate, as well as changes in human habitation and lifestyle. Some viruses, like the coronavirus (COVID-19), are potentially fatal, causing a global pandemic and leading to millions of deaths worldwide. Therefore, the development of biosensors is necessary to identify these viruses and cancers at an early stage. The book chapter aims to discuss the development of biosensors based on different device technologies (FET, AlGaAs/GaAs, AlGaN/GaN) with their performance characteristics toward biosensing applications. This chapter also focuses on two important detection techniques, label-based and label-free biosensing, and compares them with several performance factors. The performance characteristics of FET-based biosensors, AlGaAs-based biosensors, and AlGaN-based biosensors are covered in this book chapter.

Keywords: Biosensors, HEMT, Label-based detection, Label-free detection, Sensitivity, Response time.

INTRODUCTION

Over the past several years, biosensors for various applications have evolved, and extensive research has been carried out. M. Cremer, in 1906, confirmed the proportional relationship between liquid acid and electric potential. Eventually, in 1975, Yellow Spring Instruments (YSI) developed the first commercial biosensor. The first silicon-based biosensor was developed in 1980 to detect pH (Potential Hydrogen) in penicillin using the enzyme-coupled FET [1]. The FET-based biosensors will eventually be used in almost all biomedical applications to detect various cancers, viruses, tumors, *etc*. Due to its dominant features like availability, cost, and low power dissipation, silicon is the primary material for fabricating these sensing devices. Deepak Kumar Panda *et al.* recently developed

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an analytical model for negative capacitance Molybdenum disulfide (MoS_2) Field Effect Transistor biosensors to detect various DNA, proteins, and enzymes [2]. These silicon-based technologies have made biosensors competitive in the market. However, biosensors made of silicon have certain drawbacks, such as low thermal and chemical stability, poor ruggedness, being non-reusable, and being easily attacked and destroyed by chemical or biological agents. Due to these limitations, the evolution of biosensors using compound semiconductors came into existence due to their superior characteristics. Compound semiconductor materials are wide band gap materials that attract sensing platforms in environmental monitoring and medical diagnosis. Due to their superior characteristics, like high thermal and chemical stability, piezoelectric nature, non-toxicity to living cells, and high ruggedness, they are used to invent novel structures for biosensing. Heterostructures have been found to replace silicon in RF and other applications in the last 20 years. Wide band gap materials can operate in various temperatures and voltages. One of the excellent characteristics of heterostructure is 2DEG (Two-Dimensional Electron Gas) near the heterointerface. This 2DEG, in turn, increases the density of the charge carriers and mobility, hence the name HEMT. The mobility of carriers at the 2DEG interface decides the device's performance, as this 2DEG acts like a channel in a conventional MOSFET. These biosensors are modeled and fabricated using AlGaAs/GaAs and AlGaN/GaN compounds. Numerous biosensors have been developed by using these compound semiconducting materials. Compared to GaAs, AlGaN/GaN heterostructures are popularly used in biosensing for the following reasons. One of the critical advantages of GaN is its higher breakdown voltage and high power density; in addition, it has better radiation resistance. GaN devices are ideal for making smaller devices with higher speeds due to their ideal characteristics of higher bandgap and lower intrinsic concentration. GaN-based devices require less cooling and have very low weight. Due to the advantages of the GaN material mentioned earlier, researchers have moved towards developing heterostructures using AlGaN/GaN materials in various applications. The new HEMT structures are introduced to improve the performance behavior of devices. In HEMT-based III-Nitride/β-Ga_2O_3 proposed in a study, gallium oxide is used as a substrate material [3]. The effect of the spacer layer thickness of the recessed gate and field-plated III-nitride nano-HEMT on the β-Ga_2O_3 substrate is discussed in another study, showing the impact of the field plate on the performance of the HEMT [4]. G. P. Rao *et al*. proposed a Nano-HEMT based on a recessed gate structure to enhance the 2DEG channel density [5]. In a novel AlN HEMT structure proposed in a study, the gate geometry is changed to a T structure, and the authors concluded that the characteristic behavior of HEMT is similar to that of conventional HEMT with enhanced performance [6]. The Ga_2O_3 nano-HEMT structure was developed using gallium oxide; in this structure, the authors mainly

focused on engineering the gate area to improve the characteristic behavior of the HEMT [7]. A simulation model of HEMT with gallium oxide as a substrate material has better performance metrics due to its noted features when compared to the conventional HEMT [8]. In this chapter, our primary focus is on biosensing applications using AlGaN/GaN heterostructures. In order to facilitate comprehension, this book chapter is organized as follows: The introduction to various HEMTs is provided in Section 1, the discussion of biosensors is covered in detail in Section 2, the advancements in biosensing devices are covered in Section 3, and the conclusions are covered in the last section.

SENSORS IN THE BIOMEDICAL FIELD

A sensor's fundamental function is similar to that of a transducer, which transforms one type of energy into another, such as electrical to mechanical, chemical to electrical, *etc*. An analyte is a compound, whose concentration is to be measured. The quantitative analysis of different substances is measured in the analysis of a biosensor by transforming their biological reactions into quantifiable signals.

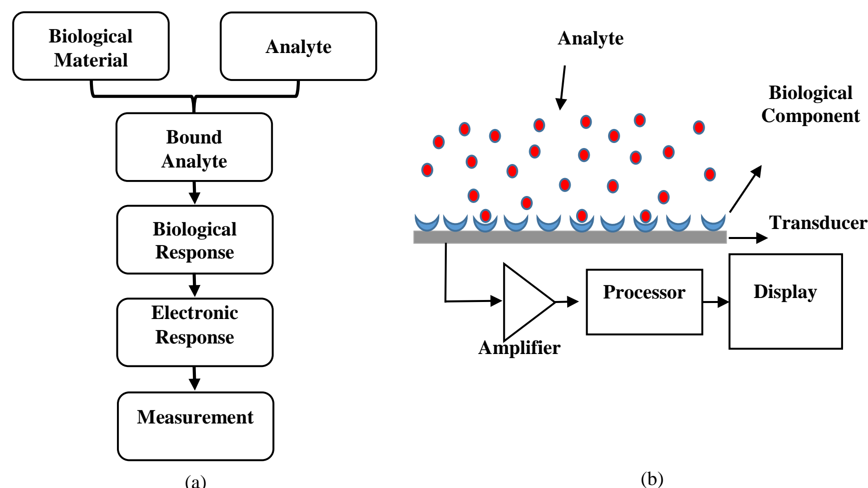

Fig. (1). (**a**) Basic Principle of a Biosensor (**b**) Physical structure.

The performance of the biosensor mostly depends on the specificity and sensitivity of the biological reaction and the stability of the enzyme. According to the fundamental idea of a biosensor, the target biological material is immobilized using a traditional technique, as illustrated in Fig. (**1a**). The detailed physical structure of the biosensor is depicted in Fig. (**1b**), along with a transducer that converts the biological signals to the required measurable electrical signals, which

CHAPTER 15

2D Material Tungsten Diselenide (WSe_2): Its Properties, Applications, and Challenges

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Abstract: In this chapter, we study the characteristics of the 2-dimensional material Tungsten Diselenide (WSe_2), along with its properties, applications, and challenges. Here, we present in detail the evaluation of TMDC materials and other 2D materials available in comparison to WSe_2 materials. We also differentiate these materials based on their qualities, characteristics, advantages, and applications in detail. Later, we discuss the designed device structure of the WSe_2FET along with its simulation results. Simulation analysis describes the input and output characteristics of a transistor with WSe_2 as channel material and compares its response with the conventional MOSFET. Thereafter, we discuss the hetero-dielectric structure performance with different high-K values, and then a dielectric-modulated biosensor device is designed to study its characteristics and sensitivity. It is observed from the analysis that hetero-dielectric structure devices have a high Ion/Ioff current ratio compared to conventional MOSFET due to high interface layers interaction and high gate controlling capability. Finally, we study the sensitivity behavior of the device and understand that as the K-value rises, the device sensitivity increases because of the high electrostatic property in nature. WSe_2 has a larger surface-to-volume ratio, which provides a larger sensing area for interactions with biomolecules, potentially enhancing the sensitivity of the biosensor.

Keywords: DMC, Graphene, MoS_2, Sensitivity, Tungsten Diselenide (WSe_2).

INTRODUCTION

In this chapter, we will study in detail the 2D material "Tungsten Diselenide" (WSe_2) structure, its properties, applications, and challenges. In semiconductor technology, scaling is the process of reducing the size of electronic devices to increase their performance and functionality by reducing cost and maintaining low power consumption. During this scaling process, we come across many SCEs

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like DIBL (Drain Induced Barrier Lowering), threshold voltage roll-off, hot-carrier effects, sub-threshold swing, velocity saturation, and so on. To overcome these SCEs, we have different methods such as channel engineering, gate engineering, the strained silicon method, multiple gate transistors, doping optimization, technology scaling with alternative materials, advanced processing techniques, and many more. The method "technology scaling with alternative materials" is based on the concept of "Nanotechnology", which describes different nanomaterial classifications and their properties. The field of nanomaterials has brought new possibilities for future technologies by exploring and harnessing the unique properties of materials at the nanoscale. Specific material properties are selected based on the desired application [1].

Nanomaterials refer to materials that have structural features on the nanometre scale, typically ranging from 1 to 100 nanometers. Because of their small size and enhanced surface area-to-volume ratio, these materials have distinct features that set them apart from their bulk counterparts. There is a wide variety of nanomaterials, and they can be classified depending on their composition, structure, and properties. Table **1** shows different terms associated with nanomaterial technology [2].

Table 1. Various terms related to nanomaterials

Terms	Description
Nanotechnology	Nanotechnology is a sort of technology that creates materials, devices, or systems at the nanoscale level by managing matter at the nanoscale length to activate the material's unique properties.
Nanomanufacturing	It refers to the fabrication of materials at the nanoscale level, which can be performed using bottom-up or top-down processes.
Nanoscale	A scale ranging from 1 to 100 nm.
Nano-object	It is a discrete piece of nanoscale material having one, two, or three exterior dimensions.
Nanoparticle	When all of the dimensions of an object or particle are in the nanoscale range, it is referred to as a nanoparticle.
Nanomaterial	A substance is considered a nanomaterial if it has at least one dimension in the 1-100 nm nanoscale range.
Nanofiber	A nano-object with two dimensions in the nanoscale range and a much larger third dimension
Aspect ratio	A nano-object's aspect ratio is defined as the ratio of the length of the major axis to the width of the minor axis.
Nanosphere	A nanosphere is a nanoparticle with a one-aspect ratio.
Nanorod	When the shortest and longest axes have variable lengths, the name nanorod is used. Nanorods have a width between 1 and 100 nm and an aspect ratio greater than one.

(Table 3) cont.....

Terms	Description
Nanowire	Nanowires, like nanorods, have a greater aspect ratio.
Nanotube	Nanotubes are hollow nanofibers.
Nanocomposite	Nanocomposites are multicomponent materials with numerous distinct phase domains, at least one of which has a dimension in the order of nanometers.

The properties of nanomaterials can differ based on their composition, size, shape, and structure. Some common properties of nanomaterials include enhanced mechanical strength, improved electrical and thermal conductivity, unique optical properties (*e.g*., fluorescence, plasmonic effects), and increased reactivity. These properties make nanomaterials highly promising for an inclusive variety of applications in fields like electronics, energy, medicine, and environmental science [3].

Materials can be divided into various dimensions depending on their structural features: zero-dimensional (0D) (for example, nanoparticles), one-dimensional (1D) (for example, nanotubes and nanorods), two-dimensional (2D) (for example, graphene), and three-dimensional (3D) (for example, nanoprisms and nanoflowers). The dimensional classification of materials provides a framework to understand and study the unique properties and applications of materials based on their structural arrangement. By manipulating materials in different dimensions, scientists and engineers are developing materials with tailored properties for specific applications [4, 5].

The classification of 2D materials is based on their crystal structures. The two main types of 2D materials are:

Single-layer Materials

These materials are made up of a single layer of atoms organized in a two-dimensional lattice. Graphene is the most well-known example of a single-layer material composed of carbon atoms organized in a hexagonal lattice.

Transition Metal Dichalcogenides (TMDs):

TMDCs materials contain the formula MX_2, where M is a transition metal (for example, Mo or W) and X is a chalcogen (for example, S, Se, or Te), which are composed of three atomic layers stacked together, forming a layered structure. The middle layer consists of a transition metal atom, such as molybdenum (Mo) or tungsten (W), crammed between two layers of chalcogen atoms, such as sulfur (S) or selenium (Se). TMDCs have a variety of crystal forms, including 1T (one-layer trigonal structure), 2H (Two-layer hexagonal structure), and 3R (Three-layer

CHAPTER 16

Memristors as Prospective Devices for Silicon and Post-Silicon Eras: Theory, Applications and Perspectives

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Abstract: Silicon-based semiconductor devices have sustained Moore's Law for a long time. However, with the downscaling of devices, the focus of the industry has shifted toward alternative materials having application-specific properties. Memristors have emerged as one of the prospective semiconductor devices for multi-faceted applications due to their data retention properties, convenient fabrication, and less complex circuit architectures. The dual resistance states of memristors have been employed in multiple intelligent applications, including brain-inspired computing architectures, methods, cryptography frameworks, and biological sensing. The non-volatility of memory and compatibility with CMOS-style architecture have led to a wide range of domains that are capable of exploiting the properties of memristors. A number of mathematical models have also been developed to explain the working principle of memristors. This chapter reviews the theory and applications of memristors for the silicon era and presents the future perspectives of these devices for the post-silicon era.

Keywords: CMOS-compatible memristors, Memristor neural networks, Memristive logic, Memristive sensors, Memristive machine learning, Neural intelligence, Silicon memristors.

INTRODUCTION

The current primary demands of the semiconductor industry have aligned toward improving the performance of specific applications rather than embedding a greater number of transistors on a die area alone. This indicates that the preference of utility shall be assigned to devices based on application-specific performance rather than average performance for multiple tasks. While silicon has remained

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the most reliable element for manufacturing on one hand, research on alternative materials for the post-silicon era has been continuing on the other. Moore's Law has been pivotal in guiding the semiconductor industry toward meeting the demands of functionalities that have grown over time. However, as the channel length in metal oxide semiconductor field effect transistors (MOSFETs) approaches the lattice dimensions, application-specific integrated circuits are given more focus to sustain the technological advancement and meet the criteria of the economics of the industry.

In the pursuit of following Moore's Law, as conventional MOSFETs begin to suffer from short dimension effects, the industry has been on the search for alternate materials and devices. Different devices have emerged and revolutionized the industry since then, targeting different applications according to their principles of operation. One of them is the two-terminal element called memristors. In the history of memristors, some claim that Humphry Davy carried out the first tests depicting memristive properties as early as 1808. The memristor (*i.e*., memory resistor), a name coined by Bernard Widrow in 1960 for a circuit part of a primitive artificial neural network dubbed ADALINE, was the first device of a similar sort to be constructed. Argall reported and demonstrated the resistance-switching properties of TiO_2 in 1968, which was later used as proof of a memristor by Hewlett Packard researchers [1]. After that, the memristor was first introduced by Leon Chua in 1971. He explained the missing link between flux and electric charge in the form of frequency-dependent characteristics of a memristor, which gives a hysteresis loop-like characteristic in its current-voltage plot [2].

The terms "memory" and "resistor" are literally combined to form the term "memristor", which functions as a resistive switch. Memristors depict hysteresis in current-voltage plots at low frequencies, but as the frequency rises, its lobe width reduces. Beyond a critical frequency, the memristor behaves like a resistor with a linear relationship between the current flowing through it and the voltage across it [2]. Resistive memristors and polymeric memristors are two classes of memristors, but the primary problem with resistive memristors is that there is no direct correlation between magnetic flux and charge; compared to resistive memristors, polymeric memristors show memristive behavior that is more consistent with Chua's prediction. Memristors have been utilized for multiple applications, like highly efficient memory arrays, resistive switching-based memory, analog amplifiers, digital circuit topologies, oscillators, neuromorphic networks, and adaptive filters [3].

The memristor, like any new technology, is frequently preferred for its potential to improve the energy efficiency, functionality, dependability, and scalability of

any existing circuit [4]. Since memristors are emerging as important electronic devices for next-generation computing systems, it is critical to explore the security and trust concerns associated with this growing technology [5]. The emergence of the memristor is driving the semiconductor technology industry toward new paradigms and possibilities for transforming circuit design, ushering in a new era of neuromorphic and analog applications and innovations. High scalability, low power discharge, CMOS-compatible circuits, and flexibility make memristors ready for application-specific designs. The prime models to characterize memristors are the Linear Ion Drift Model, Non-Linear Ion Drift Model, Simmons Tunnel Barrier Model, TEAM Model, and VTEAM Model.

In the case of memristor circuits, bipolar junction transistors (BJTs) were shown to be particularly useful since the current produced by the transistor improved the memristive performance. Memristor BJT (MBJTP) pair hybrid circuits were examined to be applied as current regulators, AC switches, variable negative resistance, and variable pulse generator [6]. Over the past decades, memristor-based memory cell design has experienced a renewed surge in interest, primarily because of its remarkable combination of high speed and minimal power demand. A unique hybrid memory cell with the least number of transistors required for quick bidirectional write operation was designed as a memory cell. One of the essential components for high efficiency and great memory performance is read stability. To create a speedier and more reliable memory cell, a memristor was added to traditional CMOS transistors [7]. The electrical behavior of a memristor is used to identify the amount of protein in various dietary products. The dual resistance states of proteins are exploited to identify proteins in various food items [8].

The applications of memristor-based Digital Signal Processors (DSPs) are mostly concerned with the enhancement of memory performance and neural network synapse formation. In the majority of the documented applications, memristor models based on mathematics are used to verify the suggested DSP circuits [9]. The development of brain-inspired computers mimicking the power usage and memory density of biological neural networks has received particular interest in recent years. In fact, the human brain is capable of performing roughly 10 quadrillion operations per second while using just 20 W of power to carry out complicated tasks like pattern association, speech recognition, and picture recognition. The level of emulation and the computational models of various neuronal types and neural processes are the dependencies of the mechanism of brain emulation [10].

The power efficiency of brain-inspired computing systems may be improved with the help of memristor-based computation. There is still a need for behavioral

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