NANOELECTRONICS DEVICES: DESIGN, MATERIALS, AND APPLICATIONS PART I

Editors:
Gopal Rawat
Aniruddh Bahadur Yadav

Bentham Books

Nanoelectronics Devices: Design, Materials, and Applications (Part I)

Edited by

Gopal Rawat
SMIEEE, School of Computing and Electrical Engineering (SCEE), Indian Institute of Technology Mandi (IIT Mandi), Kamand-175075, Mandi, Himachal Pradesh, India

&

Aniruddh Bahadur Yadav
Department of Electronics and Communication Engineering Velagapudi Ramakrishna Siddhartha Engineering College (Autonomous), Kanuru Vijayawada Andhra Pradesh - 520007 India

Nanoelectronics Devices: Design, Materials, and Applications (Part I)

Editors: Gopal Rawat and Aniruddh Bahadur Yadav

ISBN (Online): 978-981-5136-62-3

ISBN (Print): 978-981-5136-63-0

ISBN (Paperback): 978-981-5136-64-7

First published in 2023.

need for a court order if at any point you breach any terms of this License Agreement. In no event will any delay or failure by Bentham Science Publishers in enforcing your compliance with this License Agreement constitute a waiver of any of its rights.

3. You acknowledge that you have read this License Agreement, and agree to be bound by its terms and conditions. To the extent that any other terms and conditions presented on any website of Bentham Science Publishers conflict with, or are inconsistent with, the terms and conditions set out in this License Agreement, you acknowledge that the terms and conditions set out in this License Agreement shall prevail.

Bentham Science Publishers Pte. Ltd.
80 Robinson Road #02-00
Singapore 068898
Singapore
Email: subscriptions@benthamscience.net

CONTENTS

FOREWORD

The idea of studying nano-structures was established in the year 1959 when Nobel laureate and theoretical physicist Richard Feynman spoke about miniaturizing old-age computers in his famous talk entitled "There's plenty of room at the bottom". Recently, the 2016 Nobel Prize in Chemistry awarded to Prof. Jean Pierre Sauvage, Prof. Sir J. Fraser Stoddart, and Prof. Bernard Lucas Feringa "for the design and synthesis of molecular machines", established yet another key milestone in the history of nanotechnology. Nanotechnology, in recent years, has delivered innovations that have the potential to completely transform the direction of technological advances in a wide range of applications such as nano-engineering, nano-materials, nano-electronics and nano-medicine. The evolution of nano-technology is undoubtedly going to result in sweeping changes to humanity and our society. Not just limited to engineering and material sciences, the innovations in nano-technology have allowed us to come up with a logical deduction towards understanding the complex and multiple associations within biomolecules and biological systems.

This book takes us on a voyage through the realm of new discoveries and innovations in the field of nano-technology. The book consists of twenty-three chapters; each chapter addresses specific facets of nanoscience and nano-engineering involving basic concepts of physics, chemistry, biology and mathematics for the development of new products. This enthralling journey takes us through multifarious terrains of nanotechnology, such as nano-electronic products, nano-technology for electronic modules, characteristics and application of field effect transistors as sensors. In addition, it includes extensive discussion on nanomaterials applications, including but not limited to, nano-dentistry and cosmetic industry and energy harvesting using solar cells.

In light of the recent inventions, discoveries and breakthroughs in the field of nano-technology, this book promises to equally delight nano-technology researchers, students and enthusiasts.

Rahul Checker
Radiation Biology & Health Sciences Division, Bhabha Atomic Research Centre
Trombay
Mumbai 400085
India

PREFACE

In recent years, nanoelectronics devices have been finding potential applications in all fields that are easing the life of human beings, like agriculture, energy harvesting, medicine, battery, sensors, optoelectronics, pyro-photonic, food processing, bio-nanotechnology, aerospace, automobiles, pharmaceutical, paints, cosmetic, aeronautic, medical imaging (MRI, ultrasound), *etc*. Therefore, it is necessary to produce well-organized information for researchers, scholars, academicians, and scientists working on the design, synthesis, and simulation of nanoelectronics devices and simulation modeling and characterization of materials for nanoelectronics devices. This information would help those working on nanoelectronics to conduct academic classes, research, and develop new products. Industries are producing nanoelectronics devices for different applications by putting great effort into the research and development to make them more efficient, reliable, durable, and low cost, which needs systematic information on current developments in the field.

These requirements have encouraged the editors to invite proficient, learned, and expertized authors to contribute chapters and provides in-depth information and concept of present nanoelectronics devices considering material synthesis, design, and synthesis of nanoelectronics devices. The authors of chapters have worked in the field for a long time and proven themselves in their field over the globe. The chapters are classified as nanotechnology-based solar-cell, medical devices, power grid devices, agriculture devices, cosmetic biosensors, and advanced transistors. The chapters present theoretical and experimental work and broad reviews of the existing state-of-the-art. The simulation and modeling of the nanoelectronics devices and materials for nanoelectronics devices are also considered equally. This book is for a one-semester course on nanoelectronics devices. The book is classified into two volumes one and two. First volume consists fourteen chapters, those presented here.

ORGANIZATION OF PART I

Chapter 1 of the book starts with a broad introduction to nanoelectronics devices and nanomaterials, where the authors present the present, past, and future of nanoelectronics. Nanotechnology briefly introduces and applicability of MOORs law. This chapter produces the classification of the nanomaterials based on the size and different nanofabrication approaches, like top-down and bottom-up.

Chapter 2 presents the self-assembly of the monolayer for molecular electronics, an integrated part of nanoelectronics. Transport of charge carrier, electrode, and measurement of the such device covered in detail. Materials used for the fabrication of the molecular devices are also presented.

Chapter 3 presents the performance of the core cell double gate junctionless transistors for current nanoelectronics-based integrated circuits. A multigate field effect transistor properties modified by channel doping. Fermi level adjustment in junctionless transistor explained properly. In junctionless transistors, there is a core, and cell structure improves its performance.

Chapter 4 presents tunneling field effect transistors that lead to the area reduction on the integrated circuits, mostly in non-polar devices. The results are simulated for a channel length of 20 nm under varying temperatures to understand the leakage current and other transistor parameters.

Chapter 5 presents a nanowire-based field effect transistor that overcomes the limitations of the conventional MOSFET. The negative capacitance of the nanowire-based field effect transistor is explained in depth. Band bending and distribution of potential simulated and presented. The implication of transistors in integrated circuits is presented with illustrations and simulation results.

Chapter 6 discusses an electrode's effect on the linear region of a thin film transistor. The triple material double gate was applied to control current conduction in the channel, and silicon was the channel material. The three metals are arranged horizontally of varying lengths affecting the transistor performance. The transistor performance is analyzed in both analog/RF ranges.

Chapter 7 deals mechanism of gas sensing by thin film transistors whose channel is of II-IV semiconductor, an effective transistor in the current generation of technology. Novel metals improve the gas sensing properties of the bare II-IV-based semiconductor. Transistor active layers have different characteristics identified by different characterization tools: atomic force microscope, X-ray diffraction, *etc*. Electrical characteristics in hydrogen and without hydrogen are investigated.

Chapter 8 produces a wast state-of-art of fin FET important nanoelectronics. Fin FET shows high mobility of the carriers, an improvement over the double gate. Details about current conduction and control over the channel are identified. SOI further improves the properties of this transistor. New trends in Fin FET technology are also presented in detail which would help readers to do future development in existing technology. Fin FET physical structure is evaluated intensively.

Chapter 9 provides the best example of the integration of electronics and optics. Such transistors are tunneling types those explained in previous chapters. Simulation results obtained by technology computer-aided design produced. Working and geometry are explained properly.

Chapter 10 produces self-powered photodetectors, a nanoelectronics device important for optical communication applications. Single nanobelt to pyro-photonic devices are presented, and different terminology associated with these photodetectors is defined. Quantum confinement in low dimensional materials and energy level in those illustrated. The mechanism of self-powered is also appropriately explained.

Chapter 11 solar cells attracted significant attention as fossil fuel ended and the economy expanded rapidly—nanomaterials and nanostructures are producing better solar cells and increasing the energy harvesting efficiency many folds. Different crystal structures are also illustrated that decide mobility, carrier transport, band gap, and other mechanical properties of any materials—solar cells are classified in first, second, and third generation depending on material composition efficiency and structure, *etc*.

Chapter 12 introduces the lead-free solar cell based on nanomaterials. Other methods used to harvest energy are also listed and discussed. Why nanomaterials are needed in energy harvesting is also elaborated.

Chapter 13 provides information on how nanomaterials are helpful in energy harvesting. Janus Materials, Van-der-Waals Structures, Chalcogenides Materials, and Organic nanomaterials are explained. Solar cell classification is done by considering materials that will help readers to select materials for specific solar cell fabrication.

Chapter 14 detailed the hybridization potentiality of the material for energy harvesting and storage. Conversion efficiency, fill factor, short circuit current density, *etc*., are illustrated profoundly to provide an in-depth concept of solar cells. Many roots are listed to harvest energy cost-effectively. Many single solar cells connection in a solar panel are also discussed. Emphasis on electron-hole generation at the junction and transport to load. Equivalent circuits of solar cells would further enhance the reader's knowledge.

ACKNOWLEDGMENTS

Editors special thanks to almighty god for giving light to write a book on nanoelectronics devices: design, material, and application to serve scientific society. We sincerely thank all contributors, reviewers, and colleagues who made this project successful. Editor's special thanks go to Mr. B.S. Sannakashappanavar for his valuable time compiling the book in its present form. Editors also thank their M.Tech and Ph.D. students for their support while editing the book.

Gopal Rawat
SMIEEE, School of Computing and Electrical Engineering (SCEE), Indian Institute of Technology Mandi (IIT Mandi), Kamand-175075, Mandi, Himachal Pradesh, India

&

Aniruddh Bahadur Yadav
Department of Electronics and Communication Engineering
Velagapudi Ramakrishna Siddhartha Engineering College (Autonomous),
Kanuru Vijayawada Andhra Pradesh - 520007, India

List of Contributors

Abhishek Bhattacharjee	Department of ECE, Tripura Institute of Technology Narsingarh, Agartala-799015, India
Aswin Ramesh	Department of Physics, National Institute of Technology Calicut, Calicut-673601, Kerala, India
Amit Saini	Cadre Design Systems, Ghaziabad, India
Amandeep Singh	School of Electronics and Electrical Engineering, Lovely Professional University, Phagwara, Punjab, India
Ankita Saini	Department of Chemistry, P.D.M. University Bahadurgarh, Haryana, India
Anup Shrivastava	Computational Nano-Materials Research Laboratory (CNMRL), Indian Institute of Information Technology, Allahabad, India
Brinda Bhowmick	Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Assam, 788010, India
Bhavesh Vyas	Department of EEE & ECE, K.R. Mangalam University, Gurgaon, Haryana, India
C. S. Suchand Sangeeth	Department of Physics, National Institute of Technology Calicut, Calicut-673601, Kerala, India
Dharmendra Singh Yadav	National Institute of Technology, Hamirpur, Himachal Pradesh, India
Gopal Rawat	SMIEEE, School of Computing and Electrical Engineering (SCEE), Indian Institute of Technology Mandi (IIT Mandi), Kamand-175075, Mandi, Himachal Pradesh, India
Ghanshyam Singh	Department of Electronics and Communication Engineerin, Malaviya National Institute of Technology Jaipur, Rajasthan, 302017, India
Hemant Kumar	Department of Electronics and Communication Engineering, Jaypee Institute of Information Technology, Noida, Uttar Pradesh, India
Jayesh Vyas	Department of Mechanical & Chemical Engineering, Indian Institute of Technology, Jammu, India
Jaismon Francis	Department of Physics, National Institute of Technology Calicut, Calicut-673601, Kerala, India
Jyoti Kandpal	Department of ECE, Graphic Era Hill University Dehradun, Uttarakhand, India
Koushik Dutta	PDPM Indian Institute of Information Technology, Design and Manufacturing, Jabalpur, India
Lintu Rajan	National Institute of Technology, Calicut, Kerala, 673601, India
Mohit Agarwal	Thapar Institute of Engineering and technology, Patiala, Punjab 147004, India
Prajwal Roat	National Institute of Technology, Hamirpur, Himachal Pradesh, India
Prabhat Singh	National Institute of Technology, Hamirpur, Himachal Pradesh, India

Puja Acharya	Department of EEE & ECE, K.R. Mangalam University, Gurgaon, Haryana, India
Puspa Devi Pukhrambam	Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Assam, 788010, India
Rahul Ghosh	Department of ECE, Tripura Institute of Technology Narsingarh, Agartala-799015, India
Rupanjal Debbarma	Department of ECE, Tripura Institute of Technology Narsingarh, Agartala-799015, India
Sukanya Ghosh	National Institute of Technology, Calicut, Kerala, 673601, India
Shekhar Verma	Lovely Professional University, Jalandhar, Punjab, India
Sweta Chander	School of Electronic and Electrical Engineering, Lovely Professional University, Phagwara, Punjab, India
Sanjeet Kumar Sinha	School of Electronic and Electrical Engineering, Lovely Professional University, Phagwara, Punjab, India
Sunil Kumar Saini	Department of Chemistry, P.D.M. University, Bahadurgarh, Haryana, India
Sumeen Dalal	Department of Chemistry, P.D.M. University, Bahadurgarh, Haryana, India
Shivani Saini	Computational Nano-Materials Research Laboratory (CNMRL), Indian Institute of Information Technology, Allahabad, India
Sanjai Singh	Computational Nano-Materials Research Laboratory (CNMRL), Indian Institute of Information Technology, Allahabad, India
Shikha Kumari	PDPM Indian Institute of Information Technology, Design and Manufacturing, Jabalpur, India
Tanmoy Majumder	Department of ECE, Tripura Institute of Technology Narsingarh, Agartala-799015, India
Talapati Akhil Sai	PDPM Indian Institute of Information Technology, Design and Manufacturing, Jabalpur, India
Vishal Narula	Lovely Professional University, Jalandhar, Punjab, India
Vandana Devi Wangkheirakpam	Department of Electronics and Communication Engineering, Indian Institute of Information Technology Senapati, Manipur, India
Varun Goel	Department of Electronics and Communication Engineering, Jaypee Institute of Information Technology, Noida, Uttar Pradesh, India
Vineet Dahiya	Department of EEE & ECE, K.R. Mangalam University, Gurgaon, Haryana, India

CHAPTER 1

Role of Nanotechnology in Nanoelectronics

Jyoti Kandpal[1,*] and **Gopal Rawat**[2]

[1] *Department of ECE, Graphic Era Hill University, Dehradun, Uttarakhand, India*

[2] *SMIEEE, School of Computing and Electrical Engineering (SCEE), Indian Institute of Technology Mandi (IIT Mandi), Kamand-175075, Mandi, Himachal Pradesh, India*

Abstract: Nanotechnology is concerned with creating and applying materials with nanoscale dimensions in various facets of life. Additional features have been introduced to the world of electronics due to advancements in nanotechnology. The development and cost-effective manufacturing of cutting-edge components that function quickly, use less power and can be packed at much higher densities is made possible by nanotechnology's new and unique features. There is a revolution in biotechnology, food, the military, and medicine using nanotechnology.

Keywords: BJT, CMOS, ENIAC, FinFET, MOSFETs.

INTRODUCTION

Digital logic, which needs to offer a technology foundation for two different device types—high-performance logic and low-power/high-density logic—takes up a significant percentage of semiconductor device manufacture. Therefore, speed, power, density, price, capacity, and time to market are important factors for this technology platform. To preserve historical patterns of increasing device performance at lower power and cost while still operating in large volumes, the More Moore roadmap offers an enablement vision for further scaling of MOSFETs.

By European Nanoelectronics Initiative Advisory Council (ENIAC), the silicon-based micro or nanoelectronics industry can be analyzed utilizing three general categories as shown in Fig. (**1**) [1, 2].

[*] **Corresponding author Jyoti Kandpal:** Department of ECE, Graphic Era Hill University Dehradun Uttarakhand, India; E-mail: jayakandpal27@gmail.com

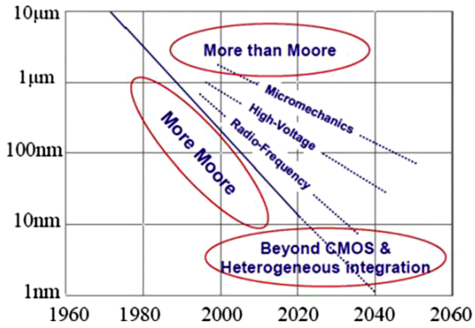


Fig. (1). ENIAC predication for microelectronics future.

1. **Advanced CMOS** (**More Moore**): To continue the downsizing of transistors, particularly in the improved use of metal gates with suitable work functions, high-k oxides, and high-k oxides as insulators, to ensure an effective throughput while decreasing the leakage *via* gate stack.

More Moore targets bringing PPAC value for node scaling every 2−3 years [3]:

a. (P)performance: >10% more operating frequency at scaled supply voltage.
b. (P)ower: >20% less energy per switching at a given performance.
c. (A)rea: >30% less chip area footprint.
d. (C)ost:<30% more wafer cost 15% less die cost for scaled die.

2. **More than Moore**: Modern CMOS technology has demonstrated itself as inherently constrained. Radiofrequency, analogue circuits, switches with high-voltage, actuators, and motion sensors are non-digital functions that call for a combination of technologies customized to a particular need. To overcome these obstacles and implement new features like mechanics, optics, acoustics, ferroelectrics, *etc*., "more than Moore" is needed.

The relevance of more-than-Moore devices, which combine performance, integration, and cost without being restricted to CMOS scaling, will continue to expand. These devices include MEMS, power electronics, CMOS image sensors, and R.F. devices. There are four standards more–than-Moore emphasizes [4].

a. System On a Chip (SoC)
b. System On a Package (SoP)
c. System In a Package (SIP)
d. Multiple Chip Module (MCM)

3. **Beyond CMOS.** New materials, whether inorganic or organic, are covered with new operating principles, such as those that replace electrons with magnetic excitation or spin and unique architectural designs. Examples of alternatives beyond CMOS include new materials for interconnects and transistors such as nanowires and carbon nanotubes, switches working with resistive change polymers for memories, the electronic properties of organic molecules, and memory and computing architectures to utilize the capabilities of these new devices fully.

The designing of electronic systems on a single chip requires optimum exploitation of "system-on-chip" devices, and it will be a vital component of the future of nanoelectronics, integrating "More Moore" and "More than Moore" with new "heterogeneous integration" technologies. Another advancement is "system-in-package", which uses different optimized process technologies for combining multiple distinct sub-systems in a single package.

WHAT IS NANOSCALE?

The word "nano" originated from the Greek word "Nanos," which means " tiny, dwarf, or exceedingly small". As per the International Systems of Units, the prefix "nano" represents one billionth or 10^{-9}. It means one nanometer is one billionth of a meter [4]. Fig. (**2**) shows the visual illustration example of nanoscale:

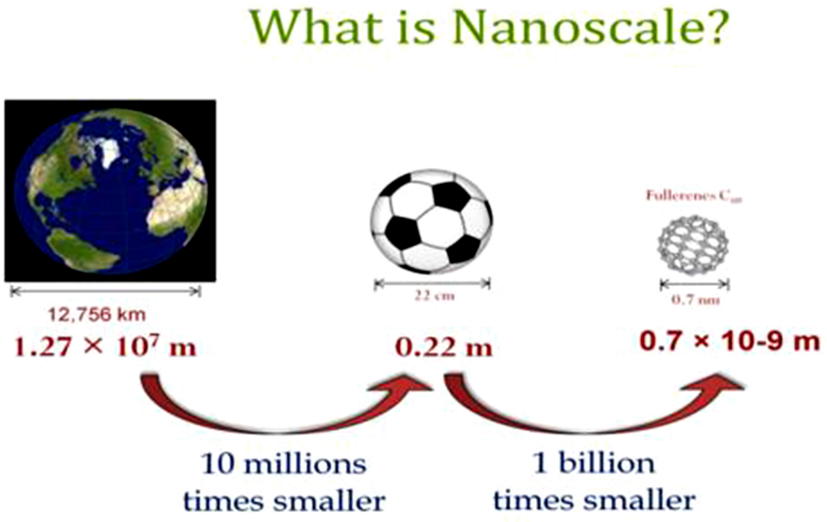


Fig. (2). A Nanometric Scale.

CHAPTER 2

Self-Assembled Monolayer-Based Molecular Electronic Devices

Jaismon Francis[1], Aswin Ramesh[1] and **C. S. Suchand Sangeeth[1,*]**

[1] *Department of Physics, National Institute of Technology Calicut, Calicut-673601, Kerala, India*

Abstract: This chapter focuses on molecular tunnel junctions (MTJ), the basic building block of molecular electronics (ME), which consist of either a single molecule or an ensemble of molecules in the form of a self-assembled monolayer (SAM) sandwiched between two electrodes. MTJs based on SAMs find practical applications such as diode rectifiers, switches, and molecular memory devices. The predominant charge transport mechanism in two-terminal junctions is tunneling; therefore, perturbances in the bond length scale will translate into nonlinear electrical responses, allowing MTJ to induce and control electronic activity on nanoscopic length scales with various inputs. For this reason, the subject is now progressing to devices based on finite ensembles of molecules, and many studies are underway to develop devices that can augment and complement traditional semiconductor-based electronics. SAM-based tunnel junctions are like single molecular junctions, demonstrating effects like quantized conductance, tunneling, hopping, and rectification; they also possess a unique set of properties. In addition, several new problems that need to be addressed arise from the unique characteristics of SAM-based junctions. General aspects of the two terminal molecular junctions, roles of the electrode, molecule, and molecule electrode interfaces, and how to differentiate the components of a molecular junction using impedance spectroscopy are discussed in this chapter. Different testbeds to measure the charge transport in SAM-based tunnel junctions are discussed, and a comparison of the reported charge transport data on alkanethiolate SAMs is presented. Finally, the molecular rectifiers are briefly discussed.

Keywords: Charge transport, Impedance spectroscopy, Molecular tunnel junctions, Molecular rectifier, Self-assembled monolayers.

INTRODUCTION

The history of electronics is well connected to the progress in the miniaturization of electronic components. For instance, the first computers were still cupboard-sized, whereas small-sized laptops available these days surpass those computers in

* **Corresponding author C. S. Suchand Sangeeth:** Department of Physics, National Institute of Technology Calicut, Calicut-673601, Kerala, India; E-mail: sangeeth@nitc.ac.in

Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

memory, computational power, and all other performance properties by several orders of magnitude. Having more transistors per chip, more sophisticated integrated circuits are realized, which eventually transformed society in an unimaginative way. Due to fundamental scaling limitations, efforts to design various new nanoelectronic devices and materials as substitutes for complementary metal oxide semiconductor (CMOS) transistors-based electronic circuits have been intensive [1]. As the dimensions of conventional semiconductor devices are pushed below 100 nanometers, it creates many fundamental and technical challenges. For example, traditional scaling methods influence vital parameters like the device's threshold voltage and on/off currents. The increased financial cost of associated equipment required to produce semiconductor devices is holding back efforts to improve the capabilities of these devices [2].

In the devices mentioned above, electronic components based on molecules are crucial. When molecules are used as the main component of electronic devices, it offers numerous degrees of freedom intrinsic to molecular structure. Tuning the electrical characteristics of the molecular devices could be easily achieved by altering the structure of the molecules. Therefore, they are a potential candidate for next-generation electrical components [1]. ME studies electron transport across one molecule or an ensemble of molecules sandwiched between two electrodes [3]. Nowadays, ME is rapidly evolving. Molecular-mechanical switches operated by single electron transfer, three-input mechanical Boolean sorter, electrically gated single molecule switches, *etc.*, are some of the milestones in this field so far [4, 5].

Aviram and Ratner's paper in 1974 and subsequent studies have shaped ME into what it is today. They suggested a single molecular rectifier having a Donor-Bridge-Acceptor construct [6]. The ultimate goal of ME is to conquer the fundamental scaling limits of conducting polymer or traditional silicon-based inorganic devices by building nanometer-sized active or passive electronic components [7]. The exciting aspect of ME is that the electronic functions exhibited by inorganic semiconductors can be mimicked by functionalizing a single molecule sandwiched between a two-terminal junction [8]. Experimental development of such a concept using a variety of methods like scanning probe microscopes, break junctions, soft metallic contact, nano transfer printing (nTP), lift-off-float-on electrodes, *etc.*, have been realized through the years [9, 10]. These solutions achieved single MTJ, exhibiting effects like quantum interference effect, quantized conductance, tunneling, hopping and rectification [11].

Reproducibility, robustness, integration, and upscaling limit the incorporation of single-molecule into practical applications. The problem lies in controlling the geometry, structure, and orientation of the individual molecules with the interface.

Due to *n* number of geometries and orientations that a molecule can have at the interface of an electrode and various defects in the junction, the measured value of current varies to a large extent. Thus, each device fabricated using the exact method and material tend to be distinguishable, posing the issue of reproducibility and making the device irrelevant. It should also be noted that there is an inherent difficulty for the molecules to be stable when subjected to an external bias. The contact resistance at the molecule/metal interface was one of the most challenging problems due to the variation in the performance of the junctions. In 1971, Mann and Kuhn performed charge transport measurements in SAMs of cadmium salts fatty acids between two metal electrodes [12]. They observed an exponential decay of the conductivity independent of temperature as the chain length of the monolayer increased, which they ascribed to incoherent tunneling through the monolayer. Molecular electronic junctions with an ensemble of molecules are statistically more favorable than a junction consisting of a single molecule due to the inconsistency in results produced by the latter. The concept of a 'finite ensemble of molecules' is realized through SAM. SAMs are ordered arrays of molecules that spontaneously form by adsorption of constituent molecules from solutions or the vapour phase [13], and Kuhn performed charge transport measurements in SAMs of alkane(di)thiol in a two-terminal configuration [12]. This was a significant breakthrough as it was later established that SAMs are a practical alternative to the electronic functionality that a single molecule offers.

ME is a broad field, and excellent reviews are available that discuss the progress of two-terminal MTJ [14]. These reviews mainly focus on materials and practical challenges in the design and fabrication of an MTJ. Our attempt is not to replicate this; instead, this chapter focuses on the methods to analyze the obtained data. We also discuss the usefulness of impedance spectroscopy in identifying the circuit elements in the junction and determining the charge transport bottlenecks in the MTJ. The device details primarily addressed in this chapter are two-terminal MTJ (molecules or SAMs of n-alkanethiols, where n is 2 to 16 sandwiched between two stationary electrodes). Although two-terminal devices are widely studied, many conflicting results can be found in the literature [13 - 15]. These contradictions arise since different groups use different electrodes or testbeds for the same molecules resulting in MTJs with different characteristics. The top and bottom electrode and the kind of interface it makes with the monolayer and the bulk of the monolayer influence the device's electrical characteristics. Recently Mukhopadhyay *et al.* conducted a cross-laboratory study to understand charge transport in protein-based junctions. In their research, they tried to answer how results from various platforms and labs can be compared and how to discern the distinction between platform-induced and true protein electrical transport characteristics [16]. Results from the study show that the effective contact area is determined by junction geometry, and the charge transport mechanism is not

CHAPTER 3

Performance Analysis of Rectangular Core-Shell Double Gate Junctionless Transistor (RCS-DGJLT)

Vishal Narula[1,*], Shekhar Verma[1], Amit Saini[2] and **Mohit Agarwal[3]**

[1] *Lovely Professional University, Jalandhar, Punjab, India*

[2] *Cadre Design Systems, Ghaziabad, India*

[3] *Thapar Institute of Engineering and technology, Patiala, Punjab 147004, India*

Abstract: The shrinking of the device parameters' dimensions could be a solution for improving the performance and high transistor density of traditional MOSFETs. However, the short-channel effects could create a problem in the performance of the device. This chapter examines and performs comprehensive simulations of the standard junctionless double-gate transistor. In this research, silicon thickness and work function engineering are used to better understand the junctionless transistor's operation. As silicon thickness increases, the junctionless double-gate FET's performance begins to decline. Additionally, the typical double-gate junctionless FET is modelled, and the change in silicon thickness, work function, gate dielectric, and doping concentration is studied. The findings of the analysis and simulation are found to be quite similar. As a result, the device is referred to as a rectangular core-shell double-gate junctionless transistor because of the core being sandwiched between the two shells of the device (RCS-DGJLT). While the core-shell is doped with acceptor impurities in an n-type RCS-DGJLT, donor impurities are used in the shells. The device performance parameters have been improved such that I_{OFF} of order ~10^{-14}A, I_{ON} ~10^{-5}A, I_{ON}/I_{OFF} ~10^{9}, SS nearly 68.9mV/decade, DIBL nearly 52.6mV/V are obtained at a total silicon thickness of 12nm and channel length of 20nm. The effect of channel length variation on RCS-DGJLT is also studied. RCS-DGJLT is found to have better performance than conventional DGJLT.

Keywords: Core-Shell, DIBL, Junctionless, MOSFET, Multigate, Oxide Material, Subthreshold-Slope, Transconductance, Threshold Voltage, VLSI.

INTRODUCTION

The development of the electronics sector is greatly stepped up by increasing consumer spending around the globe. With the increase in economies, consumer

[*] **Corresponding author Vishal Narula:** Lovely Professional University, Jalandhar, Punjab, India;
E-mail: vishal.narula2302@gmail.com

demand also increases. It was in the 20th century that the electronic industry was born. The most profitable sector within electronics is the semiconductor industry which has grown to become more than $400 billion globally as of 2018.

When Brattain, Shockley, and Bardeen built the first transistor in 1947, this revolution in the semiconductor industry began. This is followed by an introduction to the "workhorse of the electronics industry," which is the MOSFET. For the last 30 years, microelectronics which is a subfield of electronics that relates to the study of small electronic components and design, has benefited marvelously from MOSFET miniaturization. Complementary metal-oxide-semiconductor (CMOS) has revolutionized the human lifestyle. The larger packaging density and improved performance showed the supremacy of reduced physical size. According to Moore's law, the transistor density on a chip will double every 18 months, and improvements in many properties would accompany that increase.

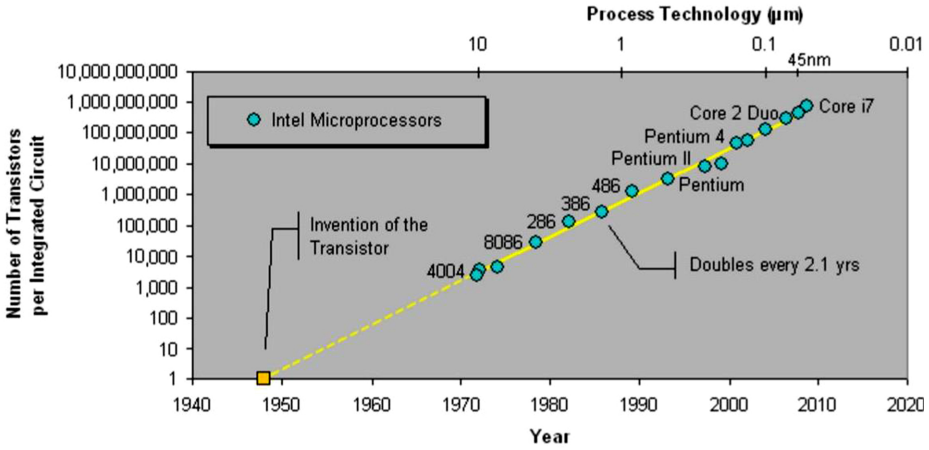


Fig. (1). Transistor density along with process technology node opted by intel microprocessors from the year of the invention of the transistor.

Fig. (**1**) shows an illustration of the number of transistors per integrated circuit and process technology node opted by intel microprocessor from the invention year of the transistor, which follows Moore's law. The latest development of an artificial intelligence (AI) chip called "Cerebras'" with 1.2 trillion transistors is now commercially available. Further, the miniaturization of dimensions of the MOSFET is becoming difficult due to short channel effects (SCE's) and higher gate leakage currents that limit the device performance, such as higher microprocessor speed, along with less power dissipation. There are various challenges during the scaling of the transistors, like gate leakage current, better gate control, output current, power/performance ratio and reliability of the device.

The challenges under gate control lie in different short channel effects, which include gate-induced drain leakage (GIDL), subthreshold slope degradation, gate oxide tunneling of carriers, source/drain direct tunneling, DIBL, which degrades the performance of the device and thus affects the subthreshold characteristics.

For further downscaling of the dimension of the MOSFET, the multi-gate-based MOSFET's (MugFET) comes into the picture such that the control on the carriers of the device can be enhanced [1]. MugFET improves the SCE's, reduces the device variability and increases the carrier mobility without the need for high doping concentration. The SCE's are highly reduced in MugFET's not by scaling the oxide dielectric but by scaling the thickness of the channel, which brings down the gate tunneling current. Therefore, due to these advantages, according to International Roadmap for Semiconductors (ITRS), MugFET's have been predicted as a successor to planar transistors since 2001 [1]. Fig. (**2**) shows different multigate device architectures. The double gate [2], triple gate [3], quadruple gate [4], cylindrical gate [5] and bulk FinFET [6] architectures are thus shown below.

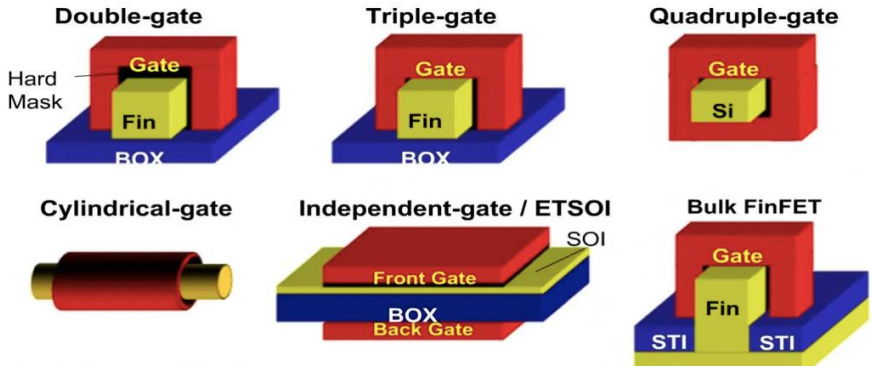


Fig. (2). Different device architectures of multigate FET.

The reduction in SCE's gives a great motivation towards achieving the best performance of the miniaturized device. Unfortunately, the presence of source and drain region does not nullify the SCE's completely in MugFET's and brings challenges in doping profile techniques. The requirement of abrupt source and drain junctions in ultra-short channel devices invites multiple complications, even in MugFET's [7]. The drain and source regions of n-type MOSFETs are extensively populated. Acceptor and donor concentrations of 10^{15} cm^{-3} and 10^{20} cm^{-3}, respectively, are used to dope the channel region. To realize such abrupt doping concentration in short-channel devices is a tedious task. The statistical nature of the distribution of dopant atoms and the law of diffusion restricts to

CHAPTER 4

Performance Analysis of Electrical Characteristics of Hetero-junction LTFET at Different Temperatures for IoT Applications

Sweta Chander[1] and **Sanjeet Kumar Sinha**[1]

[1] *School of Electronics and Electrical Engineering, Lovely Professional University, Phagwara, Punjab, India*

Abstract: Scaling down the metal-oxide- semiconductor (MOS) technology in the nanometer regime has been performed to achieve high device performance, but reliability and power consumption are the main concern for the semiconductor industry. In the past few years, area-scaled tunneling field-effect transistors (TFETs) have been researched aggressively to enhance the tunneling cross-sectional area of devices. Although the area-scaled Tfet increases the device footprint for the same channel length when compared to the conventional TFET structure. This problem can be resolved by considering a nonplanar device structure. The LTFET structure enhances the on-state current and reduces the device footprint area. In the present study, a detailed analysis of the electrical characteristics of L-shaped TFET (LTFET) through 2-D TCAD simulations is presented. The proposed hetero-junction LTFET with 20 nm gate length exhibits a high I_{ON} of 1.08×10^{-4} A/μm, low I_{OFF} of 1.57×10^{-14} A/μm, high I_{ON}/I_{OFF} of 10^{10}, and steep sub-threshold slope (SS) of 25 mV/dec at room temperature. The analysis has been carried out to encounter the effect of Gaussian traps at the channel–gate oxide interface at a wide range of temperatures from 250 K to 350 K. An extensive study on the influence of temperature variations on various DC analysis, AC analysis, linearity analysis, and electrical noise analysis has been carried out. The study reveals that the electrical parameters like I_{ON}, IOFF, and SS, on which all figures of merit (FOMs) of the device depend, show a small variation with increasing temperature. The drain current noise spectral density (S_{ID}) changes from 2.12×10^{-26} A^2/Hz to 2.42×10^{-20} A^2/Hz, and voltage noise spectral density (S_{VG}) changes from 1.79×10^{-11} V^2/Hz to 1.97×10^{-5} V^2/Hz on increasing temperature from 250 K to 350 K. The change in temperature does not impact the on-current of the device, while a small variation in the off-current occurs. The various FOMs of the device also show small variations in the results with increasing temperature. The only unfavorable factor where the evident change in the results has been observed is the electrical noise characteristics of the device. The reliability analysis clarifies that the proposed LTFET device performs well at a wide range of temperatures and can be well-suited for low-power applications.

* **Corresponding author Sweta Chander:** School of Electronic and Electrical Engineering, Lovely Professional University, Phagwara, Punjab, India; E-mail: sweta.chander@gmail.com

Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

Keywords: Noise analysis, Interface Traps, Gaussian Traps, Reliability Analysis, Band-To-Band Tunneling (BTBT), Temperature.

INTRODUCTION

The nanoelectronic industry has emerged rapidly and continuously as it merges nanotechnology in electronic components. The technological improvement in the design, use of different materials, and suitability of the device in applications motivate the growth of the nano-electronic industry [1]. The size of nanoelectronic devices ranges between 1 nm to 100 nm. The primary engine of the progress of the industry is miniaturization [2]. Scaling down the metal-oxide semiconductor (MOS) technology in the nanometer regime has been performed to achieve high device performance, but reliability and power consumption are the main concern for the semiconductor industry [3, 4]. Moreover, under the minimum fundamental limit of subthreshold slope (SS), the scaling of V_{DD} gets restricted. These issues get resolved using an outstanding device, *i.e*., tunnel field effect transistors (TFETs), that come into the scene to attain low SS [5 - 7]. The band-to--to-band tunneling (BTBT) mechanism of TFET offers steep SS and low off-state current [8]. In the past few years, area-scaled TFETs have been researched aggressively to increase the device tunneling cross-sectional area. The area-scaled Tfet increases the device footprint compared to conventional TFET of the same channel length [9, 10]. This problem can be resolved by considering a nonplanar device structure. In this study, to enhance the on-state current and reduce the device footprint area, LTFET is proposed [11 - 14].

Despite the development of different TFET structures, the effect of noise on the device performance is still not explored extensively [15 - 19]. Nonetheless, the impact of introducing traps on the effect of device performance has been reported in a few studies [20 - 24]. Ghosh and Bhowmick reported the low-frequency noise analysis in the presence of uniform and Gaussian interface traps. The improved current ratio and SS were obtained in the case of uniform traps than the Gaussian trap [25]. Wangkheirakpam *et al*. presented the effect of uniform and Gaussian traps in D-MOS TFET and discussed the effect of temperature variation on device characteristics [26]. Another simulation study of the effect of trap on oxide/semiconductor interface for different charge distribution was reported by Talukdar and Mummaneni. From the study, it has been found that the Gaussian trap degrades the device performance compared to the uniform trap in terms of current ratio and SS [27].

This chapter deals with the effect of variation on transfer, output characteristics and electrical noise behavior, linearity, and reliability of a hetero-junction LTFET device with a 20 nm gate length. The effect of the Gaussian trap on the noise

behavior of the device also has been performed. The simulation study has been carried out using the Sentaurus TCAD tool. The chapter is organized into four sections. The chapter starts with the introduction section, followed by the proposed device structure and simulation methodology. Moreover, the fabrication process flow of the proposed LTFET has been discussed in detail. Moreover, the obtained results and discussion consists of DC analysis, AC analysis, linearity analysis, electrical noise analysis, and reliability analysis. Finally, the study has been concluded by discussing the important findings and the future scope of the proposed device.

DEVICE STRUCTURE

Fig. (**1a**) depicts the schematic of the proposed TFET along with the device dimen- sions used for the simulations. In n-type TFET, the P++ region is defined as the source region of Ge doped with a boron concentration of $1\times10^{19}cm^{-3}$. While the N++ region is defined as the drain region of Si with a phosphorous concentration of $1\times10^{19}cm^{-3}$. An offset region with a boron concentration of $1\times10^{15}cm^{-3}$ has been created to enhance the TFET performance. The channel is doped with a boron concentration of $1\times10^{15}cm^{-3}$. The offset region is a channel region, as both are doped with the same concentration. The height of the offset region is optimized as it is the tunneling junction, and the maximum tunneling of charge carriers occurs in the offset region. A 2 nm thick HfO_2 with a dielectric constant of 22 is used as the gate oxide, while Al, with a work function of 4.3, is used as the gate metal. The calibration of simulated data is done with the experimental data to verify the accuracy of the simulation set-up [28]. Fig. (**1b**) depicts that the obtained data is in good agreement with the experimental data, hence it validates the selected models.

PROPOSED SIMULATION FRAMEWORK

All simulations have been carried out in Sentaurus TCAD [29]. The TCAD tool works with an algorithm to determine the nonlocal BTB tunneling rate without prior knowledge of tunneling locations [30]. The TCAD models used for the simulations are summarized in Fig. (**2**).

CHAPTER 5

Device Structure Modifications in Conventional Tunnel Field Effect Transistor (TFET) for Low-power Applications

Amandeep Singh[1], Sanjeet Kumar Sinha[1] and **Sweta Chander[1,*]**

[1] *School of Electronics and Electrical Engineering, Lovely Professional University, Phagwara, Punjab, India*

Abstract: With the rapid scaling of transistors in the nanometer regime, various short-channel effects emerge in short-channel devices; researchers are looking for an alternative device to replace complementary MOSFET (CMOS) in circuit applications. TFETs are considered to be a good replacement for the conventional MOSFET in the upcoming technologies. The methods used for making I_{ON} higher also impacts the I_{OFF} current. So, the overall current ratio remains unaltered. To overcome this problem, a technique has been developed and adopted in this work that not only improves the current ratio but also makes the subthreshold swing steeper. The major improvements are the reduction of short channel effects, enhancing current ratio reducing dynamic power consumption. Negative capacitance being a new phenomenon, helps in providing improvised results. The device optimized in this work has given values of Subthreshold swing as 53.75 mV/decade, I_{ON} and I_{OFF} as $4.295*10^{-5}$ A/μm, $6.01*10^{-15}$ A/μm, respectively. DIBL calculated for conventional NCTFET is 61.2 mV/V, and for proposed NCTFET is 31.92 mV/V. So DIBL improvement of 52.2% has been achieved.

Keywords: Complementary MOSFET, Current ratio, Drain Induced Barrier Lowering (DIBL), I_{ON}, I_{OFF}, Negative Capacitance, Sub-threshold swing, Tunnel Field Effect Transistor.

INTRODUCTION

With the continuous scaling of transistors, the channel length of semiconductor devices so formed is causing serious problems with regard to current ratio, subthreshold swing, and leakage current. In the new age devices, the channel is becoming shorter, making the channel length the same as the depletion width of the drain and source junction. Other short-channel effects such as mobility degra-

* **Corresponding author Sweta Chander:** School of Electronics and Electrical Engineering, Lovely Professional University, Phagwara, Punjab, India; E-mail: sweta.chander@gmail.com

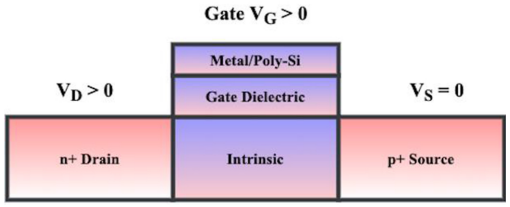
Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

dation, drain-induced barrier lowering (DIBL), and drain punch-through have also been introduced in devices with short channels. The researchers are now adopting various alternate device structures to replace the MOSFET device with an improved and better device incorporating the latest device modifications and structures [1]. The new-age devices presented in the literature are successful in achieving better device performance and overcoming the short channel effects, which in turn, provide promising results for low-power applications [2].

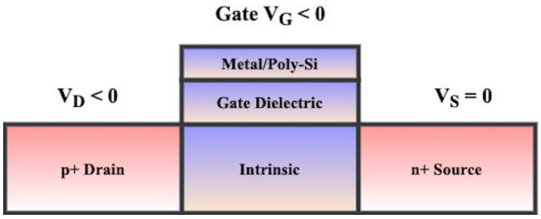
According to Moore's law, the density of transistors (*i.e.*, the number of transistors) roughly doubles every two years. It gives a historic trend and provides an estimate of future requirements. The next important parameter that demands attention is Power consumption. The most common solution to higher power consumption is to choose a lesser supply voltage but there is an upper limit to this. After a specific value of threshold voltage (V_{TH}), it restricts the further downfall of supply voltage [3]. V_{TH} voltage depicts the lowest value below which the transistor will not operate. Device structure modifications also have a direct impact on power consumption and device characteristics. Conventional MOSFET has been replaced by new-age FET devices, such as Nano Wire Field Effect Transistor, Carbon Nanotube Field Effect Transistors (CNTFET), Tunnel Field Effect Transistors (TFET), L-Shaped TFET, U-Shaped TFET, *etc.* to overcome the problem of leakage current and less stepper subthreshold swing.

TFET STRUCTURE AND ITS WORKING PRINCIPLE

Tunnel field effect transistor (TFET) consists of PIN structure (*i.e.* p-type, intrinsic, n-type). It is similar to conventional MOSFET but source and drain terminals are of opposite biasing and the electrostatic potential of the intrinsic area is controlled by the gate voltage. When the gate voltage is applied to the intrinsic region of the TFET, the electron buildup takes place. When this applied voltage crosses the threshold, band-to-band tunneling occurs as the conduction band of the intrinsic region comes in line with the valence band of the P-region as depicted in Fig. (**1**). This in turn is responsible for the current flow in the device. As soon as the gate bias reduces, the bands disalign, making the device turn off [4]. Due to its ability to provide a higher current ratio and stepper subthreshold swing, TFET can act as a good option to be utilized in low-power applications in place of conventional MOSFET. Moreover, as TFET is dependent on a band-t--band tunneling mechanism, it provides i) lesser I_{OFF}; ii) Cuts high fermi energy tail; and iii) I_{ON} current is controlled by tunneling area and width [5]. With the advantage of lowering the SS slope below 60 mV/dec and achieving a better current ratio at a lesser supply voltage, TFET can effectively be used in practical circuit applications.



(a)



(b)

Fig. (1). Supply voltages in case of (**a**) n-TFET (**b**) p-TFET.

By incorporating a germanium source, a much lesser I_{OFF} current is achieved as compared to a conventional MOSFET device, which has a direct impact on power consumption (dynamic as well as static). The major shortcoming of using TFET is the ambipolarity and lesser I_{ON} current. These limitations can be overcome by using new-age device architectures and choosing the materials wisely [6]. Fig. (**2**) shows the schematic diagram of Conventional TFET.

Concept of Negative Capacitance: Applied to TFETs

Due to the continued demand for high-performance devices, the power dissipation of devices is also increasing. This is leading to serious problems, such as reduced reliability, higher weight, increased operating cost, *etc.* Nowadays, researchers are looking for alternate low-power techniques to overcome the listed problems. As reported by Giovanni in 2007, the Negative capacitance phenomenon intervened by using the Fe layer is the main factor associated with lowering subthreshold slope in NCFET transistors. Another advantage of negative capacitance is better voltage amplification and a higher current ratio [7]. Salahuddin and Datta [1] presented in their work that the dynamic power of the device can be reduced by replacing the insulating material with ferroelectric material in conventional

CHAPTER 6

Impact of Electrode Length on I-V Characteristics to Linearity of TFET With Source Pocket

Prajwal Roat[1], Prabhat Singh[1,*] and **Dharmendra Singh Yadav[1]**

[1] *National Institute of Technology, Hamirpur, Himachal Pradesh, India*

Abstract: In this chapter, the author demonstrates a triple metal double gate TFET with a uniformly doped source pocket (TMG-SP-DG-TFET) to investigate the impact of triple metal length variation (Length of an electrode implanted above the oxide region) on the device performance. When the electrode length near the drain and source region varies, the electrostatic potential and electric field near the source-channel (SCi) and drain-channel interface (DCi) may vary accordingly. Due to these deviations, the tunneling improves or reduces for a moderately doped drain and a highly doped source region. Therefore, the I_{ON} (ON-state current) has shown significant functionalities with electrode length variation. This extensive study was carried out for the investigation of analog parameters, including EBD (ON/OFF state), E_{field}, Potential, g_m (Trans-conductance), C_{gs} and C_{gd} (Gate-to-source and Gate-to-Drain capacitance), Maximum cut-off frequency (f_t), Gain bandwidth product (GBP), Transit Time (τ), with Linearity figure of merit that includes, g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, IMD_3, and 1dB compression point. This comprehensive study shows that varying the length of the metal electrode with a fixed doping level of the source pocket will improve the overall performance of TMG-SP-DG-TFET.

Keywords: BTBT (Band-to-band-tunneling), EBD (Energy-Band-Diagram), Work-function (WF), Capacitance, Electric field (E_{field}), Linearity FOMs.

INTRODUCTION

Metal oxide semiconductor FETs play a vital role in laying the foundation of electronic industries with a backbone in transistors. The advancement in technologies allows users to have more functionality, a high-speed device, and low supply voltage with low power dissipation. However, MOSFETs have limitations like low subthreshold swing, high leakage current, and high power dissipation. This problem should be considered to improve device efficiency, and that is where Tunnel FETs come into the picture [1 - 3]. Therefore, TFETs are regarded as an alternative to MOSFETs with high sub-threshold swing and low

* **Corresponding author Prabhat Singh:** National Institute of Technology, Hamirpur, Himachal Pradesh, India; E-mail: prabhat@nith.ac.in

Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

leakage when it comes to aggressive downscaling of the device. But as for TFETs, it has limitations like low I_{ON} and high ambipolar conduction (I_{amb}) [4 - 7]. For TFETs, when it comes to I_{ON} current, it is decently equated to MOSFETs due to lessen BTBT at SCi (source-channel-interface). Henceforth, it is necessary to suggest a TFET design with a high I_{ON} current and overcome the restraint of TFET in various aspects comparable to high ambipolar current/behavior [8 - 10]. Regarding this, various engineering techniques are explored for similar double-gate TFETs (DG-TFET) [11 - 17], lower bandgap materials in source area [18 - 22], DG-TFETs with hetero-oxide, high-k dielectrics in gate oxide, Multiple gates over oxide region, *etc* [23, 24]. With the high-k dielectric material of higher permittivity, the leakage current of the device is reduced, and metal gates simultaneously screen the electrons to the high-k material [25].

In TFETs, the introduction of more than two gate designs leads to improved electrostatic control of the potential over the channel section leading to an effective increase in the tunneling region. Thus, it directly leads to an overall improvement in the I_{ON}. The combined effect of multiple gates and double gate TFETs with source pockets helps enhance the general state of the device [26 - 32].

SIMULATION DATA WITH DEVICE SPECIFICATIONS

The graphic of the TMG-SP-DG-TFET is exhibited in Fig. (**1**). It comprises the triple metal gate with hetero-Oxide of high-k oxide (HfO_2 and SiO_2) as a gate dielectric. The device is founded on silicon with the uniformly doped region of drain, channel, source, and source pocket. The n-type drain doping (N_D) is $5\times10^{18}cm^{-3}$, channel (N_C) is $1\times10^{17}cm^{-3}$, p-type source doping (N_S) set to 1×10^{20} cm^{-3}, p-type source pocket 1×10^{18} cm^{-3} correspondingly. The device parameters are enumerated in Table **1**. The length of dual metal gates (L_{SE}, for M_1 and M_3) varies for 12nm, 15nm, and 18nm while keeping the middle metal gate (M_2) constant at 20nm, with work function varying from 4.0eV to 4.8eV for M_1 (Highest WF_{M1}), M_2 and M_3 (Lowest WF). The sum of M_1 and M_3 is set to 30nm. The performance analysis of the device has been studied and equated with this carried out work concerning linearity and analog constraints of the device.

DETAILS AND EQUATIONS OF ANALOG/RF FOMS

The explanation of analog/RF variables is the main focus of this section, like gate Capacitance ($C_{gg} = C_{gd} + C_{gs}$), g_m, GBP, f_t, transit time (ô), Transconductance Generation factor, and Frequency Product (TGF and TFP) with the mathematical equations.

$$C_{gd} = \frac{\partial Q_S}{\partial V_{gs}} \quad \textbf{(1)}$$

$$C_{gs} = \frac{\partial Q_s}{\partial V_{gd}} \quad \textbf{(2)}$$

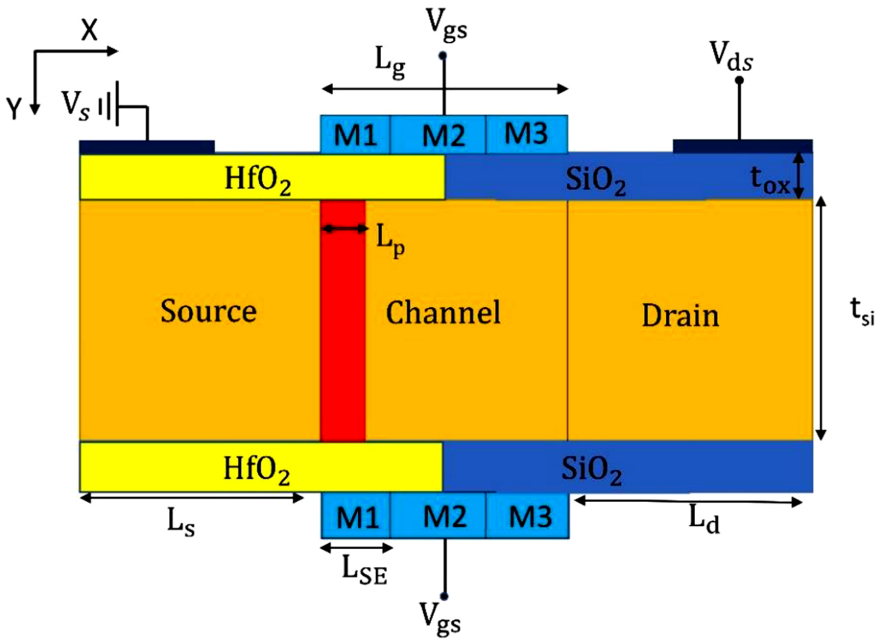


Fig. (1). Graphical illustration of TMG-SP-DG-TFET.

Table 1. Summary of simulation design variables.

S.No.	Parameters	Abbreviations	Values
1.	Gate-Length	Lg	50 nm
2.	Source-Length	L_S	100 nm
3.	Drain-Length	L_D	100 nm
4.	Source-Pocket-Length	L_P	5 nm
5.	Source-Doping-Level	N_S	10^{20} cm^{-3}
6.	Drain-Doping-Level	N_D	5 x 10^{18} cm^{-3}
7.	Channel-Doping-Level	N_C	$10^{17}cm^{-3}$
8.	Source-Pocket-Doping	N_P	10^{18} cm^{-3}
9.	Gate WF (M1)	WF_{M1}	4.2 eV
10.	Gate WF (M2)	WF_{M2}	4.8 eV
11.	Gate WF (M3)	WF_{M3}	4.0 eV

CHAPTER 7

II-VI Semiconductor-based Thin-Film Transistor Sensor for Room Temperature Hydrogen Detection From Idea to Product Development

Sukanya Ghosh[1,*] and **Lintu Rajan**[1]

[1] *National Institute of Technology, Calicut, Kerala, 673601, India*

Abstract: Implementing gas sensors incorporating nanoelectronic devices to detect pollution and improve the safety control of industrial, medical, and domestic sectors has opened up a novel world with immense interest. As a promising renewable energy carrier and a potential replacement for fossil fuels, there is the paramount importance of hydrogen gas storage at extensive facilities worldwide. The sustainable production of hydrogen is increasing owing to its enormous energy per mass of any fuel. Nevertheless, due to its extreme flammability, simple and highly accurate sensors with promising sensing materials are required to detect the slightest traces of timely leak detection for developing a hydrogen economy. Various hydrogen detectors already exist, but expensive cost, large size, sluggish response, and high temperature limit their potential for widespread applications. The integral objective of the present chapter is to focus on a systematic investigation of Pd-Ti/ZnO Schottky TFT-based room temperature hydrogen sensors excluding any heating element. With high chemical and thermal stability, ZnO is a promising candidate for sensors in a hazardous atmosphere. The developed sensor exhibited room temperature detection with a maximum response of 33.8% to 4500 ppm H_2 in dry air. The selectivity analysis toward H_2 in the presence of other reducing and oxidizing gas species has also been investigated to ensure the real-time applicability of the sensor. Reliable operation of the sensor in a wide range of 500 ppm to 4500 ppm H_2 has been confirmed from the linear behavior of the sensor. The hydrogen sensing mechanism of the proposed sensor in terms of Schottky barrier height reduction at the interface of Pd-Ti/ZnO has also been detailed in this chapter. Room temperature detection of the hydrogen sensor presented here competes favorably with the existing studies. This study can be extended in exploring new routes to realize hydrogen sensing applications at room temperature for commercialization with precise control over film thickness and target gas concentrations.

Keywords: Hysteresis, Room temperature, Pd-Ti/ZnO Schottky TFT, hydrogen sensor, Repeatability, Selectivity, Reproducibility.

[*] **Corresponding author Sukanya Ghosh:** National Institute of Technology, Calicut, Kerala, 673601, India; E-mail: gsukanya66@gmail.com

Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

INTRODUCTION

Nanoelectronics, the core foundation of next-generation electronic science and technology, has emerged rapidly and vigorously in recent years owing to various possible applications. In addition, nanosensors, particularly gas sensors composed of nanomaterials, have made increasing developments due to their dramatic advantages and specific surface states. Variations of physical or chemical properties of several gases are transformed into standard electrical signals through a gas sensor in the field of gas analysis and safety applications. In this regard, the extending demands for hydrogen sensors are not only restricted to industrial process control and environmental welfare but also extend to glassmaking, metal smelting, space flights, propulsion fuels, coal mines, nuclear reactors, petroleum extraction, semiconductor manufacturing, food, medical and chemical industries, *etc* [1 - 3]. The importance of hydrogen as a clean energy source was strongly recommended at the Conference of Parties in Paris in 2015. National Renewable Energy Laboratory in the U.S published a document concentrating on hydrogen-specific application domains [4]. There are growing demands for carbon dioxide-free hydrogen vehicles worldwide. Broadly combustible concentration range (4%-75%), high burning velocity, high ignition heat (142 kJ/g H_2), low combustion energy (0.017 mJ), large diffusion coefficient (0.61 cm_2/s), colorless, odorless, and tasteless nature are some of the several inherent characteristics of hydrogen. The mixtures of hydrogen and air are highly flammable. Hence, accurate and timely leak detection of hydrogen is essential and the need of the hour during hydroge production and storage in industrial and domestic sectors [5, 6].

However, existing solutions based on the concepts of the electrochemical, optical, acoustic wave, and calorimetric undergo the drawbacks of higher operational temperature, poor lifetime, slow response, large size, costly fabrication, design complications, high dissipation of power, and so on. FET-based gas sensors incorporating their respective electrical characteristics have been widely investigated in recent years to overcome such barriers [7, 8]. The sensing layer is the heart of a gas sensor. In this context, metal oxide semiconductors for example, TiO_2, SnO_2, V_2O_5, WO_3, Nb_2O_5, *etc*., have been broadly employed as sensing layers in FET-based gas sensors due to their noticeably reasonable cost, reduced fabrication complexities, high sensing response, lower dissipated power and quick response time. ZnO, an n-type semiconductor, has been extensively used as a hydrogen sensor. It possesses several advantages, *e.g*., the high bandgap energy (3.37 eV at 300 K), high mobility, huge exciton binding energy (60 meV at 300 K), higher thermal conductivity (116 Wm-1K-1), superior chemical and thermal stability, near UV emission, strong surface adsorption potential, d10 electronic configuration, and so on [9, 10]. Such properties ensure ZnO is a spectacular material for gas sensing. Several gas adsorbing sites determine a gas sensor's

performance; hence, a high surface-to-volume ratio sensing element is favorable. Nanocrystalline materials ensure a high surface-to-volume ratio compared to bulk. Exposure of the surface increases with decreasing crystal size. There is also an increment of a fraction of atoms at the grain boundary with reducing crystal size. Surface conductivity increases with the increasing number of nodes at the surface. ZnO is bio-safe and bio-compatible. The hexagonal wurtzite structure and a high degree of flexibility of ZnO in growth geometries are popularly investigated in sensing characteristics at minimum processing temperature. ZnO thin film associated (Pd/ZnO/p-Si and Pd/ZnO/Zn) efficiently selective hydrogen sensor is reported in the literature with 2000-20,000 ppm H_2 concentration [11]. A maximum 7.8% sensing response is achieved by synthesizing a porous ZnO thin film using the sol-gel technique to detect 250 ppm CO at 350°C [12]. Pd/ZnO Schottky diode-based hydrogen sensor is investigated by incorporating sol-gel techniques and thermal evaporation at RT [13]. Mainly produced from the zincite mineral, the ionicity of II-VI compound semiconductor ZnO falls at the borderline between ionic and covalent semiconductors [14]. It should be noted that ZnO thin films have been deposited by several methods, including CVD [6], plasma-enhanced CVD [15], spray pyrolysis [16], a sol-gel technique [17], plasma laser deposition [18], *etc*., for gas sensing applications. Although each method has its advantages, several issues still need to be overcome that may affect their gas sensing function. These relate to their poor repeatability, high synthesis time, and high operating temperature. RF sputtering is one of the best thin film deposition techniques. The advantage of this specific technique relates to uniformity in thickness, high purity, and high deposition rate; therefore suitable for large-area deposition, better controllability of deposition parameters, lower substrate temperature, and excellent film adhesion [19]. In sputtering, the material to be deposited forms the target electrode. Upon introduction inside the vacuum chamber, an inert gas, *e.g*., argon, is ionized through an electron beam. These high-energy ions bombard the target electrode and remove the target material. A vapor composed of positively charged ions is created. These vapor atoms are then deposited, covering the substrate required to be coated. RF magnetron sputtering uses magnetic fields to trap electrons in front of the target so that ionization of the inert gas increases, allowing for increasing deposition rates. At each cycle of RF sputtering, the target material surface is cleaned by the charge formation process as the electrical potential gets altered. When the positive cycle arrives, the target material comes under negative bias as electrons attract it. Striking of the target electrode continues during the negative cycle of the RF sputtering process. RF sputtering can sustain lower pressure requirements throughout the chamber. As a result, the target material can be efficiently deposited due to the lower collisions of ionized gases. Also, plasmas are usually scattered throughout the chamber instead of localizing around the target electrode. RF sputtered ZnO thin film-

CHAPTER 8

FinFET Advancements and Challenges: A State-of-the-Art Review

Rahul Ghosh[1], Tanmoy Majumder[1], Abhishek Bhattacharjee[1,*] and **Rupanjal Debbarma[1]**

[1] *Department of ECE, Tripura Institute of Technology, Narsingarh, Agartala-799015, India*

Abstract: A review of the electrical and physical characteristics of FinFETs is presented here. This work focuses on the latest structures of FinFET according to its classifications and three-dimensional schematics. Through studying the output I-V characteristics, the transfer characteristics, and the subthreshold current in the FinFET channel, the electrical characteristics of FinFETs have been analyzed. Considerations were made of coulomb, phonon, and surface roughness scattering to examine effective charge carrier mobility in the FinFET channel. Lastly, in this chapter, the impact of the Fin layer shape on device performance is studied.

Keywords: Body-tied FinFETs, Drain-induced barrier lowering (DIBL), Electromigration, Fin-height, FinFETs, Matthiesen's rule, Phonon scattering, Short channel effect (SCE), Sub-threshold slope, Spacer length.

INTRODUCTION

The FinFET structure is multigated and non-planar. With its back and front gates, the effect of the shorter channel length can be better controlled. Therefore, double-gated devices are suitable for low-power applications, since they enable a substantial reduction of reserve power while enhancing efficiency. Condensed channel impacts result from electrons floating in the direct and changing voltage caused by the contraction of channel lengths. SoI gadgets have a meager silicon film that prevents the off-state current (I_{OFF}) from flowing. It is necessary that the thickness of the silicon film is less than one-quarter of the length of the channel.

If we take HEMT (High Electron Mobility Transistor) as a counterpart of FinFETs, gate leakage is an important factor that influences their quality and presentation. By using a Gate oxide, MOS-HEMTs (Metal Oxide Semiconductors

* **Corresponding author Abhishek Bhattacharjee:** Department of ECE, Tripura Institute of Technology, Narsingarh, Agartala-799015, India; E-mail: abhishek89.187@gmail.com

Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

High Electron Mobility Transistors) can be made with improved Gate contact shape, a lower Gate current and a higher channel current. However, this results in a somewhat lower transconductance due to the larger Gate to channel detachment. A coordinated circuit's transistor count duplicates like clockwork, as Moore's law would have it. In the past, CMOS technology has been downsized using a variety of methods. This can be seen in multi-gate transistors. In a single gadget, MOSFETs are multi-gate transistors with more than one gate. As long as the cutoff and productivity are adequate, FinFET can be a fruitful apparatus. Current flow is reduced when high-κ dielectrics are used [1 - 15]. A MOSFET double gate device requires a different assembly method than a MOSFET single gate device, as shown in Fig. (**1**), which illustrates a schematic view of FinFET with geometric boundaries, such as Gate length (L_g), gate oxide thickness (t_{ox}) *etc*.

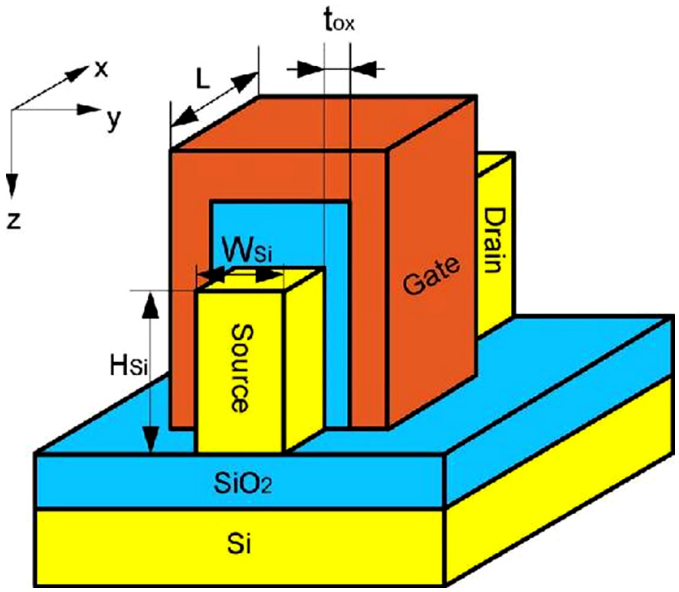


Fig. (1). Planar dimensions of FinFET [1].

On the nanometer scale, it may well be assumed that metal gates and high-κ dielectrics perform reasonably well. Due to their lower parasitic capacitances and robustness against random dopant behavior, double-gate FETs and tri-gate FETs are more appropriate for multi-gate devices [1 - 3]. Despite the reduced fringe capacitances, tri-gate FETs are complicated to fabricate. With less power consumption, immunity to SCE's, lesser area requirements, and a faster rate of operation, FinFETs are devices of choice in this era. There are several works available in the literature regarding the implementation of digital and analog circuits using symmetric and asymmetric FinFET structures. Although FinFETs

cover most of the design hierarchy, many circuit-level implementations remain untouched. As a type of Multi-gate Field Effect Transistor (MGFET), FinFETs have been granted as one of the best devices for substituting bulk MOSFETs because of their improved slope, better stability, higher on-off current (I_{ON}/I_{OFF}) ratios, superior short-channel performance, and small intrinsic gate capacitances. In terms of SC characteristics, FinFET transistors with double gate (DG FinFET) and tri-gate gates have shown standard performance. These pros can be attributed to (i) thin Si-films, (ii) lighter doping of channels and (iii) double gates for better control of channels. Researchers can use this paper to evaluate FinFET devices and understand what changes are likely to happen in the next few years based on an in-depth understanding of FinFET technology and technical issues. Also relevant to the book chapter are the failure modes and reliability of FinFETs. For several generations into the coming future, High-Performance logic will continue to use FinFET architecture. The circuit design world is rapidly maturing as new materials are being introduced, and new devices like FinFETs are bringing significant changes to the circuit design industry.

ANALYSIS OF PHYSICAL ASPECTS OF FINFET

It was mostly in the later half of the 1990s and early 2000s that FinFETs were being made on SOI wafers, or basically SOI MOSFETs. It was mostly on SOI substrates that double-gate transistors were first demonstrated to overcome the short channel effects (SCE). Due to their shallow trench isolation (STI) process and absence of leakage paths adjacent to the junction depth, these devices are renowned for their easy fabrication and excellent scalability. The doping, Si film thickness, and conditions of bias of floating body SOI devices may affect floating body problems. Compared to bulk-Si wafers, SOI wafers are more costly and have a higher defect density [4 - 6]. It is important to note that the thick buried oxide in SOI FETs has a very low heat transfer rate, preventing the generated heat of the channel from dissipating into the substrate region. With an SOI FinFET, one can also switch from a conventional four-terminal (4-T) MOSFET to a three-terminal (body floating) device, as opposed to a conventional planar MOSFET. As a result, the three-terminal characteristics narrow the operating windows. Due to this, four-terminal FinFETs, which are connected directly to Si substrates, would be more appropriate. A bulk-Si FinFET with four terminals is called a body-tied FinFET or preferably a bulk FinFET. When they were initially reported, body-tied FinFETs were termed omega (Ω) MOSFETs because the cross-section of the body was similar to the Greek letter (Ω). When reported in 2002 *IEDM, F-L Yang et al.* coined their MOSFET as the *omega FET* since the gate structure was similar to the Greek letter Ω. Body-tied FinFETs were therefore called bulk FinFETs to separate them from SOI FinFETs and omega FETs. The fin bodies of bulk FinFETs and SOI FinFETs are floated separately and anchored to the

CHAPTER 9

Optically Gated Vertical Tunnel FET for Near-Infrared Sensing Application

Vandana Devi Wangkheirakpam[1,*], Brinda Bhowmick[2], Puspa Devi Pukhrambam[2] and **Ghanshyam Singh[3]**

[1] *Department of Electronics and Communication Engineering, Indian Institute of Information Technology Senapati, Manipur, India*

[2] *Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Assam, 788010, India*

[3] *Department of Electronics and Communication Engineering, Malaviya National Institute of Technology Jaipur, Rajasthan, 302017, India*

Abstract: This chapter presents a vertical tunnel FET (VTFET) designed for light sensing application to use in medical diagnosis and treatment, tracking of targets, analysis of the chemical composition, surveillance cameras, *etc*. Various aspects related to this optimized VTFET photosensor are analyzed to benchmark its performance among those available in the literature. A brief discussion on the conventional TFET geometry is presented to give a better understanding of the advantages of its working methodologies. The concept of sensing using optically gated VTFET is studied with a remarkable focus on design perspective and detection principle. The modified TFET geometry has a photosensitive gate called an optically gated VTFET to use in near-infrared sensing applications. The design approach based on Synopsys Technology Computer-Aided Design (TCAD), along with suitable physics-based models of simulation, is introduced in this chapter. A wavelength range of 0.7μm to 1μm is considered in the simulation process. Analyses of different sensing parameters, such as sensitivity, responsivity, *etc*., at low intensity of illumination, are brought to light with the main focus on the viability of the proposed sensor to be a superior one. Through such analysis, this chapter presents a low-power, highly sensitive, cost-effective, faster response time photodetector that may be applicable for next-generation photosensors.

Keywords: TFET, Tunneling, Photosensor, Wavelength, Near-infrared light, Illumination, Sensitivity.

[*] **Corresponding author Vandana Devi Wangkheirakpam:** Department of Electronics and Communication Engineering, Indian Institute of Information Technology Senapati, Manipur, India; E-mail: vannawang46@gmail.com

Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

INTRODUCTION

In modern times, sensors are omnipresent. Without automation, life would have been very difficult [1, 2]. A sensor may be defined as a device that converts one signal into another form that can be measured more conveniently, perhaps more accurately [3]. It receives a different form of signals, *i.e*., physical, chemical and biological signals and transforms into electrical or optical signals [4]. The classification of sensors is done on the basis of the nature of the input, mechanism of conversion, applications, and various characteristics of the sensor, such as cost, range of detection or accuracy, properties of detection, *etc* [5]. There is an increasing demand for low-power, highly sensitive, faster response time, and low limit of detection optical sensors. Some commonly used photodetectors are photodiodes with PN junction, Avalanche photodiode, PIN photodiodes, FET-based phototransistors, *etc*. The presence of an intrinsic layer restricts the PIN diodes from using in applications involving high sensitivity [6]. Quantum efficiency is low in PN junction photodiodes, and Avalanche photodiodes are more prone to noise. Hence, FET photodetectors are favored over other photodetectors because of their CMOS compatibility and capability of downsizing [7]. But, the continued scaling down of the state-of-art MOSFETs experiences a power crisis problem; an issue arises due to the thermal limit of subthreshold swing (60 mV/dec). Moreover, after reaching its scaling limit, MOSFET induces short channel effects, limiting the device's performance. As a result, exploring advanced devices having steeper subthreshold slopes becomes a primary approach [8].

In recent years, many industries and researchers have proposed various devices whose working principle is different from the state-of-art MOSFETs [9, 10]. Band-to-band tunneling FET (TFET) promises a steeper SS since its current transport is governed by the tunneling of carriers from the valence band of the source to the conduction band of the channel instead of the thermionic emission as in the case of MOSFET [11]. An aggressive threshold voltage scaling can be performed in Tunnel FET, and thus it can provide a steeper sub-threshold swing (SS) [12]. However, the drain current ratio (I_{ON}/I_{OFF}) of TFETs is typically lesser when compared with MOSFETs as their ON state current depends on the tunneling probability [13]. Important research in developing the TFET from its primitive structure to its modern-day forms has been carried out to improve I_{ON} by adopting structural modifications as well as emerging materials [14]. TFET also shows another issue of current conduction in both negative and positive gate bias, known as ambipolar conduction. Till now, different modified TFET architectures having enhanced characteristics have been reported [15]. Some of the structures extensively used in the literature for various analyses include SOI TFET, hetero-junction TFET, nanowire TFET, gate-all-around TFET, dual metal gate TFET,

circular gate TFET, *etc*. TFETs are very popular for their low-power digital circuits and memory applications [16]. In the recent past, the use of TFET in sensing has become a topic of interest. The application of TFET as a dielectric modulated label-free biosensor is widely studied for its higher sensitivity characteristics [17]. The implementation of TFET in a photo-sensing application is also emerging research and is yet to explore. This sensor can be used for the detection of visible to infrared wavelengths. A photosensitive n-type Si gate separated from the channel region by a dielectric behaves as an optically activated gate upon illumination of light depending on the charge carrier excited by a photon that is accumulated at the interface. This photogating technique is adopted to look after the conducting nature of the channel using the gate field or voltage induced by light [18]. The variation in the channel conductance due to the illumination of light in the gate causes drain current fluctuation, and the change is measured in terms of sensitivity [19].

Section 2 of this chapter discusses a brief survey of some of the works reported on FET-based photosensors. In Section 3, a review of the concept, geometry and working principle of conventional TFET is presented. Section 4 mentions the principle of optically gated tunnel FET technology. Section 5 studies the sensor design and near infra-red light detection process of vertical tunnel FET-based photosensor using the photogating effect. Different sensing parameters of VTFET photosensor are defined in Section 6. The conclusion of this chapter and the comments on the future scope are presented in Section 7.

BRIEF SURVEY

Optical sensors designed using Silicon (Si) have been widely produced for optical sensing applications as they are readily available in nature, occupy less volume, and possess a good signal-to-noise ratio. In 1990, Mishra *et al*. designed an optically controlled ion-implanted GaAs MESFET and found that the electron-hole pair generation due to the incident photon flux significantly produced a drain current higher than the current generated by ion-implantation only [20]. A. Jain *et al.* proposed a high sensitivity photosensor based on Cylindrical Surrounding Gate Metal Oxide Semiconductor Field Effect Transistor (CSG MOSFET) [21]. The sensitivity parameter was measured by studying the change in subthreshold current due to the substantial increase in conductance on being exposed to light. Enhanced photo-sensing characteristics can be obtained by utilizing advanced MOSFET geometries. However, P.S. Gupta and his group designed a novel optoelectronic transistor using band-to-band tunnel FET for the detection of multiple spectral lines at near-infrared spectrum ranging between the wavelengths 0.7μm and 1μm [22]. They made use of the steeper slope advantage of TFET and obtained a better spectral response, which could resolute spectral lines that are

CHAPTER 10

Self-Powered Photodetectors: Fundamentals and Recent Advancements

Varun Goel[1,*] and **Hemant Kumar**[1]

[1] *Department of Electronics and Communication Engineering, Jaypee Institute of Information Technology, Noida, Uttar Pradesh, India*

Abstract: This chapter focuses on the evolution of Self-powered Photodetectors, from single nanobelt to highly sophisticated Pyro-phototronic effect-assisted devices. The essentials of the self-powered photodetector, from material characterization to device engineering mechanism, are discussed in detail, such as Pyro-phototronic enriched devices. This study provides a state-of-the-art research trend of the Pyro-phototronic enriched self-powered photodetectors. Finally, a summary of various device structures with their figures of merit and conclusions, along with the research gap, is presented. This review focuses on providing valuable insights into improving self-powered photodetectors.

Keywords: Pyroelectric Effect, Pyro-phototronic Effect, Quantum Dots, Self-Powered Photodetector, Solution-Processed, ZnO.

INTRODUCTION

In today's era, imaging systems [1] and sensors make human life convenient. These systems do utilize photodetectors for their operation.

Applications like spectroscopy (study of light-matter interaction) [2], weather forecasting [3], remote farming [4], forest monitoring, astronomy (analysis of the universe) [5], self-driving vehicles [6], and night vision [7] utilizing infrared radiations are based on photodetectors only. Eye spy is a trending application that mimics the human eye for IoT-based applications [8].

Photodetectors discriminate among the photons of different wavelengths conditioned over the material's bandgap. High bandgap materials (> 3eV) like ZnO [9], TiO_2 [10], GaN [11], *etc*. sense UV radiations, while small bandgap materials (< 1eV) like PbS [12], PbSe [13], HgCdTe [14], InSb [15], *etc*. are uti-

* **Corresponding author Varun Goel:** Department of Electronics and Communication Engineering, Jaypee Institute of Information Technology, Noida, Uttar Pradesh, India; E-mail: varun.goel@jiit.ac.in

Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

lized to sense IR radiations. The materials that help visible light sensing are CuO [16], Cu_2O [17], Sb_2SeTe_2 [18], CdSe [19], *etc*.

In traditional working mechanisms, reversed-biased junctions are utilized for photodetection applications. Reverse-biased junction results in a wider depletion region and allows more light to fall over the depletion region. Suppose the incident photon's energy is higher than the material's bandgap; the photon imparts its energy to the covalent bond and generates electron and hole pairs after breaking the covalent bond. If the photon energy is less than the bandgap energy, then there is no generation of electron and hole pair resulting in the transmitted photon. The separation of charge carriers represents the external quantum efficiency of the detector achieved using an electric field set up by the external reverse potential.

The photodetection process can be picturized in four steps: optical absorption, charge excitation, charge separation, and charge collection, as shown in Fig. (**1**).

Fig. (1). Four steps of photodetection flow.

The working of the photodetector, as specified in Fig. (**1**), goes through the different losses associated with the operation of the photodetector are picturized as shown in Fig. (**2**) and discussed below:

Optical Loss: Some of the light incidents on the photodetector's surface are reflected, and some are transmitted through the photodetector. These reflected and transmitted components of light contribute to optical losses. To minimize the optical losses, anti-reflecting coatings and active layers are applied according to the wavelength of interest [20].

Thermalization Loss: This is the excess bandgap energy loss in the form of heat. This loss can be minimized using quantum dots and multilayer photodetectors [21].

Recombination Loss: The photogenerated charge carriers should be collected before energy loss or recombination. The generated charge carriers are limited by the lifetime and characteristic length of the device. These losses can be minimized by electron-transport and hole-transport layers. The transport layers are highly doped n-type and p-type semiconductors, which facilitate the collection and transport of charge carriers by improving the internal electric field across the photoactive area.

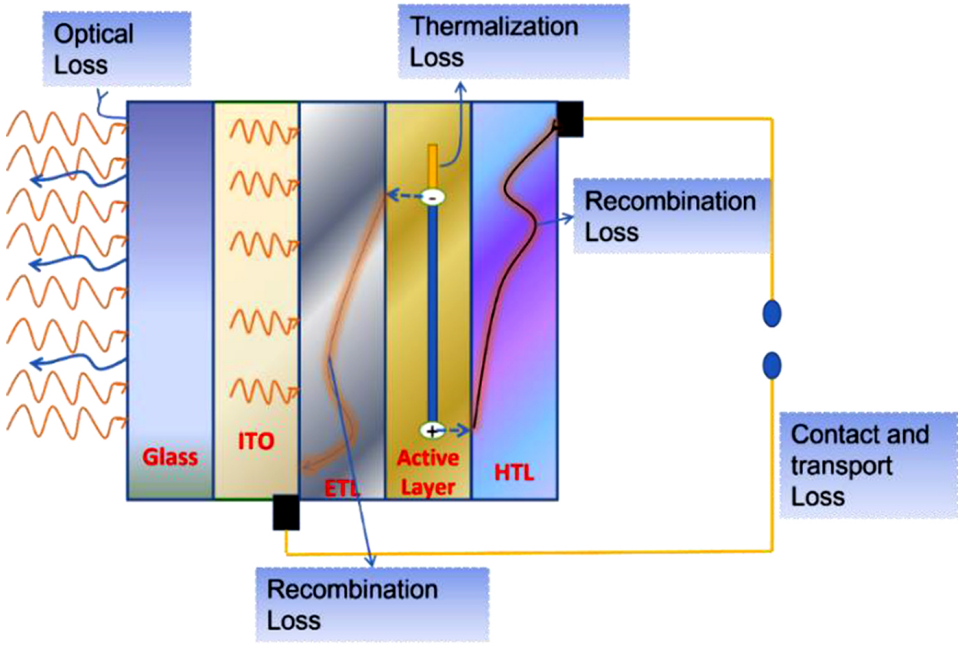


Fig. (2). Different losses associated with the Photodetector.

Contact and Transport Loss: These losses occur because of the resistance offered by contact paste and connecting wires. These losses can be minimized by using high-quality contact paste and low-resistance connecting wires.

The selection of materials for hole-transport-layer (HTL), electron-transport-layer (ETL), active area, and electrodes plays a vital role in the abovementioned losses. The performance of the photodetector accompanying these losses is generally characterized using the figures of merit, which are decided over the following parameters:

i. **Bias Voltage (volts)**: In a photodetector, a reverse bias voltage is used to implement the high electric field across the photoactive area required to separate the generated charge carriers [22]. It is desired that the applied bias voltage should be as low as possible to increase the device's viability for energy-saving applications.
ii. **Sensitivity**: Sensitivity defines the ability to detect the weak signals generated from the source. It is the ratio of current due to photogenerated electron-hole pairs (I_{ph}) to the current due to thermally generated electron-hole pairs under dark conditions (I_{dark}). The sensitivity of the photodetector should be as high as possible.

CHAPTER 11

Nanostructured Solar Cells as Sustainable Optoelectronic Device

Ankita Saini[1,*], **Sunil Kumar Saini**[1] and **Sumeen Dalal**[1]

[1] *Department of Chemistry, P.D.M. University, Bahadurgarh, Haryana, India*

Abstract: Owing to the strong interest in sustainable and renewable energy in the past recent years, the solar cell industry has grown vastly. Conventional solar cells are simply not efficient enough and are expensive to manufacture for large-scale electricity generation. There are potential and sustainable advancements in nanotechnology that have opened the door to the production of efficient nanostructured optoelectronics. Nanotechnology has depicted tremendous breakthroughs in the field of solar technology. Nanomaterials and quantum dots (QDs) have proved to be potential candidates in the field of solar cells. Nanotechnology is able to enhance the efficiency of solar cells, meanwhile helping in the reduction of manufacturing costs. Photovoltaics (PVs) based on inorganic, organic, and polymer materials are designed and synthesized with the aim of reducing cost per watt, even if it declines reliability and conversion efficiency. Such PVs absorb sunlight more efficiently with wider absorption spectra which also show better conversion of power to efficiency. Herein, we have highlighted nanoparticles based on inorganic, organic, or graphene-based functional materials, which exhibit enhanced physicochemical properties along with excellent surface-to area ratio to be used as nanostructured thin layers coated with solar cell panels. Utilizing nanotechnology in developing low-cost and efficient solar cells would help to preserve the environment.

Keywords: III Generation Solar Cells, Nanomaterials, Nanotechnology, Optoelectronics, Photovoltaics, Renewable Energy, Sustainable Environment.

INTRODUCTION

The design, synthesis, and fabrication of functional materials as well as their use in various solar applications, are areas of study in the field of materials science. In recent years, nanosized polymers, nanoparticles, and carbon-based materials have been widely investigated and used as semiconductors in electronic applications such as nano-structured photovoltaics in place of conventional inorganic Silicon-

[*] **Corresponding author Ankita Saini:** Department of Chemistry, P.D.M. University, Bahadurgarh, Haryana, India; E-mail: ankitasaini53@gmail.com

Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

based photovoltaics (PVs). To address the growing global interest in energy usage, we need to develop an alternative approach and depart from conventional methods for capturing limitless and solar energy. In elaboration on the title of the book, in this chapter, we will discuss and highlight the importance of nanostructures in solar cell technology as nanostructured optoelectronic devices. A large pool of nanoparticles is being utilized in various nanostructured electronic innovations like light emitting diode (LED), dye-sensitized solar cells (DSSC) [1], organic solar cells (OSC), and sensors which renders their helpful electronic properties, for example, charge versatility, thermal, electrical stability, luminescence and film thinning capacity. From traditional inorganic microstructured solid-state devices to nanostructured devices, they offer the primary flexibility of semiconductors which considers the incorporation of different functionalities in molecules with the help of simple molecular and structural engineering. For more than the most recent 50 years, in nanoelectronics, compounds have been examined in the field of material science [2].

Solar cells are devices which light discharge electric charges so they can move unreservedly in a semiconductor and eventually course through the formation of electricity. They work on the principle of the photovoltaic effect where "photo means light and voltaic means electricity". The wavelength useful for conversion to electricity lies within the UV-visible range, 200-800nm (Fig. **1**). But all incoming light cannot be converted by solar cells into energy because some light gets out of the cell. It is known that energy is lost in the form of heat when it is greater than the band gap energy. However, if these excited electrons are not still captured, they will immediately recombine with the holes created at the interface, and the energy will be lost. A solar cell contains a layer of p-type Si which is kept close to the layer of n-type Si. The power acquired from PV is managed by area and type of material, sunlight's wavelength and its intensity; single crystal Si solar cells are limited to the conversion of 25% of solar energy into electricity.

The photovoltaic parameters of solar cells decide what will be the IPCE (Incident photon conversion efficiency) of the solar cell. Once the device is fabricated, analysis and characterization of the solar parameters are carried out. The parameters obtained from photocurrent voltage (*J-V*) estimation under reproduced daylight are IPCE. There are 3 photovoltaic parameters:

a. "Short circuit photocurrent density (J_{SC})"
b. "Open circuit voltage (V_{OC})"
c. "Fill factor (FF)".

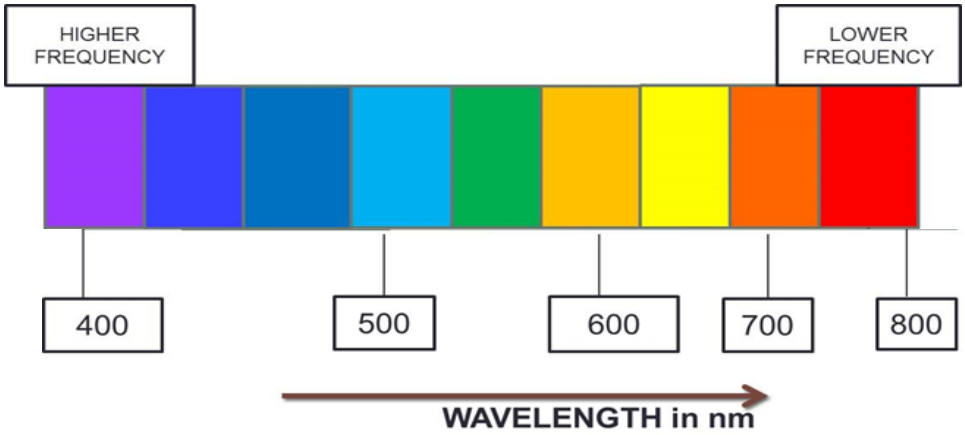


Fig. (1). Visible light spectrum.

With AM 1.5 illuminations and under standard circumstances of 100 mW/cm^{2,} *i.e.*, P_{in}, efficiency (η) of a cell can be calculated as:

"$\eta = (J_{SC} \times V_{OC} \times FF)/ P_{in}$" where FF is described as maximum power output, which is calculated from the equation "$FF = (J_{max} \times V_{max})/ (J_{SC} \times V_{OC})$".

There are 3 different types of solar panels available for usage in PV systems.

1. Monocrystalline

2. Polycrystalline

3. Amorphous thin film

Fig. (**2**) illustrates the 3 different types of solar panels available. The differences between these 3 types of panels lie in the expense and efficiency of the panels. Compared to mono-crystalline or polycrystalline solar panels, thin films, solar panels are less effective and have shorter lifespans. In contrast to crystalline solar panels, their costs are considerably cheaper because of the straightforward manufacturing processes. Modification is possible in thin-film solar panels to make them flexible, however, crystalline solar panels are rigid, brittle, and difficult to alter. Thin film panels are not advised for use in home solar systems due to their lower efficiency. To produce a certain amount of electricity, a user will require thin-film solar panels than a crystalline solar panel and hence require more area for its installation. Hence, these thin film solar panels are easily and frequently employed for commercial applications than by residential users.

CHAPTER 12

Nanomaterials Applicability in Blended Perovskite Solar Cells: To commercialize Lead-free Content, Including Easy End of life Management in Solar Infrastructure

Bhavesh Vyas[1,*], **Jayesh Vyas**[2], **Vineet Dahiya**[1] and **Puja Acharya**[1]

[1] *Department of EEE & ECE, K.R. Mangalam University, Gurgaon, Haryana, India*

[2] *Department of Mechanical & Chemical Engineering, Indian Institute of Technology, Jammu, India*

Abstract: This chapter provides insights about the Perovskite type of Solar Cell (PVSC) that can be utilized as a probable substitute for existing solar panels. Pros of reduced lead participation in chemical structure and better end-of-life supports have boosted research explorations. Combinatorial-based explorations in perovskites have created a collection of various chemical designs with unique properties and improved functionalities. Investigations in terms of catalytic nature, environment adaptability, and spintronic properties provide vivid structural arrangements. But still, constraints based on application-specific composition, raw material utilization, problems of stability issues, and the reduction in lead content are the objectives yet to be achieved at the commercial level. Interlinking of chemical structural, the nature of multiple layers created for building the material can be improvised with nanomaterials integration as detailed in the chapter. Comparative lab results analysis and efforts over raised stability and reduced lead content are taken into the study to present PVSC as upcoming commercialized products. Moreover, future scope briefs about existing nanomaterials composites with improvised electron and hole transport layers. Also, findings related to back electrode-based placement to achieve better efficiency and stability are submitted to reveal suitable obtains of the experiments covered in the study.

Keywords: Interface Recombination, Responsivity, Atomic Layer Deposition, Deposition Sequence, Chromophore, Photostability and Photocatalytic activity, Work Functions, Plasmon Resonance, slip flow, Nucleation Promoter, thickness tailoring, Quantum Confinement effect.

[*] **Corresponding author Bhavesh Vyas:** Department of EEE & ECE, K.R. Mangalam University, Gurgaon, Haryana, India; E-mail: tonu567@gmail.com

Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

INTRODUCTION

Technological changes are the research upgrades that always occur over a while. After introducing new research and innovation, big targets and challenges of making zero carbon emissions require a significant impetus from each domain.

The present book deliberates on the role of nanotechnology in various fields. Similarly, this chapter relates the upcoming modifications in the sizeable solar infrastructure market. From the solar energy point of view, conventional silicon crystals have always faced challenges in providing fabricated products at lower rates. Building crystals and weighted panels require higher temperature facilities that all include the running, operating, and summation of all types of cost, which makes it expensive. Suppose the same conditions are compared with perovskite-type solar cells (PVSCs). In that case, it sounds more reliable as perovskites can be prepared at a laboratory scale with low/average temperatures. Chemical components handling based on accuracy is required with the desired knowledge. They can be fabricated on thin films, and among all, with better power conversion efficiency compared to conventional setups.

Creating suitable perovskite is selecting the right ingredients; the rest are the procedural step. Possibilities available are nearly half a million; based upon suitable atomic configurations, the testing arrangements of precursor, additive and thermal feasibility are acquired. A random search could have an infinite loop as multiple combinatorial constraint satisfaction applied to them.

ARTIFICIAL INTELLIGENCE-BASED SCALING UP OF THE SOLAR MANUFACTURING SECTOR

The PVSC's group identified a possible upcoming replacement of the existing conventional silicon construction. Replacing the earlier practices of high-degree wafers enrichment and conversion to crystalline structures through room temperature-based fabrication setup, having fewer contingencies converted to costing over the constraints of placing and installing are considered. But still, the way to market is half done.

In the present world, the blending of algorithms has improved the results, and similar practices will be preferred in the upcoming time. Creating PVSCs utilizes multiple changing parameters that may vary concerning creation practices. Hence, machine learning will aid the work by boosting the fabrication facility. As the commercial platform is considered, the E-level of 18.5% is achieved with specific prerequisites, the work proposed by Tonio Buonassisi *et al*. [1]. Structural layering, the composition is considered for PVSCs. There are multiple numbers of combinations based on compounds concerning structural design exists. Moreover,

the creation facility need not depend only on the spin coating type of process. New practices to create better products from lab standards are still a part of experimentation. Substitute techniques are also used in rapid spray plasma processing, vacuum deposition, rolling surface ways, *etc*. It will be improvised for better outcomes in the upcoming time. Better obtaining of precursor inks on jet and spray-type techniques for roll-to-roll platforms. Time processing in the building of the silicon frame also acts as a constraint. In the case of PVSC's, it depends upon various parameters that need to be controlled with the help of machine learning. Conditions such as structure finalized, moisture, and temperature [2] . Identification of toxin-categorized elements can be submitted for data sets so that actual materials that need to be excluded can be categorized [3].

GAPS IDENTIFIED FROM THE INTERNATIONAL PROGRESS OF PVSC'S

Large-sized market cap of entrepreneurs is aimed at PVSC-based outlets globally, such as Microquanta has set up the world's first pilot manufacturing facility for perovskite products with a size of 5 GW capacity. GCL New Energy followed them up with a 100 MW-volume PVSC production setup in Kunshan. Market survey invokes that deploying an 18% efficient PVSC module can reduce 70% of the production cost of making conventional silicon PV's. The research study at Oxford PV achieved an efficiency of 29.52% in tandem structures added by Berlin's 125 MW- production setup [4, 5]. In the outdoor power generation segments: Wonder, Solar Limited fabricated printable film-type modules with a panel area of 110 m^2 are also running. [6 - 8].

The companies need to update and pass the testing/regulations in 2020. Microquanta company cleared the stability test in which a 20 cm^2 perovskite module underwent a 3000-hour damping heat test without degradation and provided an efficiency loss of less than 2% after a UV preconditioning test over a product lifetime of over 25 years. Utmo Light Ltd. followed a similar direction by passing IEC tests with a stabilized efficiency of over 20%. Recently, the Okinawa Institute of Science and Technology Graduate University (OIST, Japan) reported over an 1100-h operational lifetime for a 10×10 cm^2 solar module. Global data suggest the upcoming value of count from 84 to higher in solar cell-based startups such as:

Swift Solar in solar devices from the United States produces high power to weight share devices in the efficient PVSC field. They also utilize the ink of perovskite in energy-related services. Swedish Algae Industry – diatom frustules added dye-Sensitized based PVSCs made from algae in the direction of cell creation. Targets are set initially to raise the efficiency level to 4% higher than the present-day

CHAPTER 13

Nanomaterials and Their Applications in Energy Harvesting

Anup Shrivastava[1,*], **Shivani Saini**[1] and **Sanjai Singh**[1]

[1] *Computational Nano-Materials Research Laboratory (CNMRL), Indian Institute of Information Technology- Allahabad, India*

Abstract: The rapid advancement in technologies and a surge in the global population with the swift Industrialization led to severe challenges in fulfilling global energy demand. In the last few decades, researchers have been fiercely looking for the development of sustainable energy sources to achieve the goal of carbon neutrality and green energy generation. Among the various approaches to green energy generation, solar and thermoelectric conversions are the most lucrative. In both solar and thermoelectric means of energy generation, direct conversion of sunlight and temperature gradient into useful electricity is possible without involving heavy mechanical instruments or hazardous gases, which makes it more robust and prone to environmental degradation. Despite the several advantages, solar cell and thermoelectric power generation are still suffering from the challenges of low power conversion efficiency and long-term stability. In 2004, graphene was discovered, ushering in a new age of 2D materials research. The family of two-dimensional materials has been intensively explored in recent years as a reliable and effective alternative material for numerous applications, including thermoelectric power conversion and solar cell components, due to their distinctive material features. Geometric symmetry has a big impact on the electrical characteristics of 2D layered nanomaterials because they are highly sensitive to structural perfection. Numerous nanomaterials have recently been exfoliated, and computational predictions have been made for their potential applications in solar cells and thermoelectric generators. In this chapter, we will basically discuss the insight of emerging nano-materials, their key properties, and applications for designing renewable energy devices. The ultra-thin layer-based solar cells and nano-materials-based thermoelectric generators will also be introduced as a section of the chapter. The concept of emerging classes of nano-materials such as Janus monolayers, van-der Waals structures, and group-IV chalcogenides further piques the interest of the reader to learn about the different perspectives of nano-materials and nano-devices.

Keywords: 2D Materials, Optoelectronic Materials, Thermoelectric Generators (TEG), Solar Cells Nanomaterials, FoM, Energy harvesting, Janus Materials, VdW structures.

[*] **Corresponding author Anup Shrivastava:** Computational Nano-Materials Research Laboratory (CNMRL), Indian Institute of Information Technology- Allahabad, India; E-mail: rse2017002@iiita.ac.in

Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

INTRODUCTION TO NANOMATERIALS

With the advent of technological growth and rapid industrialization, device dimensions are shrinking to ultra-small scales called nano-scales. Nanotechnology has revolutionized almost all fields of science, such as physics, chemistry, life sciences, engineering, photonics, *etc*. The idea and concepts of nano-sciences were started and popularized by a famous scientist of the late 20th century, Prof. Richard Feynman, in his talk entitled "There's plenty of rooms at the bottom," presented on December 29, 1959, at a conference of the American Physical Society at the California Institute of Technology (CalTech). During his presentation, Professor Feynman described how science would be able to regulate and govern specific atoms and molecules. Initially, people were not much connected with his ideas, until 1981, when a German and Swedish scientist invented the Scanning tunneling microscope (STM) at IBM Zurich. With the STM, scientists are able to see and manipulate individual atoms with high precision. In the meanwhile, Prof. Norio-Taniguchi of Japan, who was experimenting with high-precision machining methods, originally used the word "Nanotechnology" in 1974 to describe the processes of atom- or molecule-scale separation, deformation, and consolidation of materials [1]. Almost after twelve years (in 1986), an American scientist Kim Eric Drexler unintentionally used the phrase linked to nanotechnology to describe what would subsequently be recognized as molecular nanotechnology (MNT) [2] in his book "Engines of Creation: The Coming Era of Nanotechnology". Afterward, the last decades of the 20th century and the beginning of the new century came with some promising breakthroughs in the nano-regimes. Now, nano-technologies are being developed for extensive uses in biomedical, electronics, energy storage, and generations, water treatments, plasma physics, space technologies, *etc*. Owing to its extremely high precision and high accuracy, nano-sciences emerged as a key concept for all branches of science and engineering.

Nanomaterials are indispensable components of nanotechnology. Materials with at least one dimension smaller than 100 nanometers are generally referred to as nanomaterials. The manipulation of matter at the nanoscale (1–100 nanometers) length and the exploitation of noble characteristics and phenomena formed at this scale lead to the production of useful nanomaterials, devices, and systems. Owing to the change in the surface area (from micro to nano) due to nanostructuring results in an alteration of the physical, chemical, thermal, and morphological qualities of the materials. Henceforth, it has been observed that the materials are producing superlative performances at the nanoscale. It is also worth noting that, without altering the chemical makeup, it is feasible to change the basic characteristics of materials by patterning matter on the nanoscale.

Nanomaterials are found to be tremendously useful in all aspects of societal challenges, such as biomedical applications, implants, wearable electronics, IoT, energy harvesting, spintronics, data storage, water treatments, smart skins, and defense applications. Some of the key application areas of nanomaterials are supercapacitors, hydrogen toys for cars, and thermoelectric generators/coolers, as shown in Fig. (**1**). In this chapter, we will focus our discussion on the various aspects of energy harvesting techniques using nanomaterials.

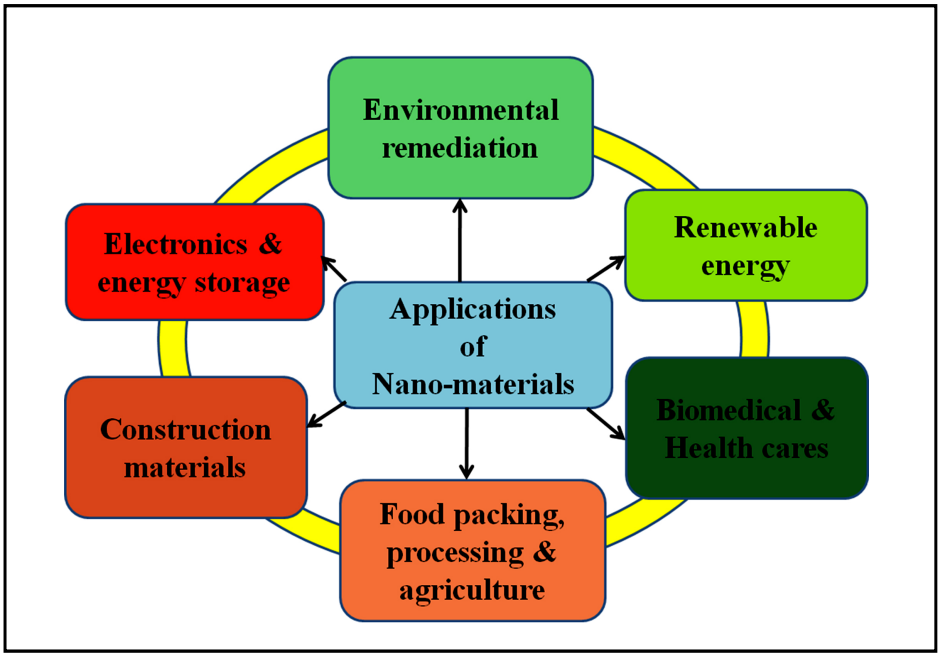


Fig. (1). Various applications of nanomaterials.

ENERGY HARVESTING

What exactly is energy? It is described as power obtained *via* the use of physical or chemical resources, particularly to give light and heat or to operate machinery. Energy is nothing more than a power that may be used to light things up, run machines, or accomplish anything else. Energy cannot be generated nor destroyed; it can only be moved from one form to another. Energy should be produced first and then stored for later use.

People have been using and storing energy in different forms since the beginning of civilization, but it attracted widespread consideration only after the industrial revolution in the 18th century. As machines and technologies have become prominent in day-to-day life, the demand for energy has also increased manyfold

CHAPTER 14

Nanotechnological Advancement in Energy Harvesting and Energy Storage with Hybridization Potentiality

Shikha Kumari[1], Talapati Akhil Sai[1] and **Koushik Dutta[1,*]**

[1] *PDPM Indian Institute of Information Technology, Design and Manufacturing, Jabalpur, India*

Abstract: Decaying sources of non-renewable energy (fossil fuel) turned the research focus to other natural renewable resources. Among these, solar power is advantageous in terms of area and maintenance cost. However, the high installation cost of conventional solar cells restricts individual uses; alternatively, lightweight and flexible solar cells evolved. Among them, Dye-Sensitized Solar-Cell (DSSC) are inexpensive and considered nanotechnological advancement. Step-by-step improvisation of the photo-conversion efficiency has been discussed in light of nanoengineering on metal oxides. Simultaneously, the dependence of wavelength on the choice of dye has also been focused opting for a particular application field. Energy storage device (solid-state batteries and/or supercapacitors) is an inevitable part of solar-cell for ensured use at required time and space. With the help of nanotechnology, the major problems of storage efficiency are critically pointed out with possible way-out. In this connection, the adopted nanoengineering aspects are extensively discussed considering improvements in the battery capacity, cycle life, and charge and discharge cycles with the highest degree of safety. Linking with the nanostructures, the nanotubular array provides a higher specific surface area maximizing the performance for both the DSSCs and energy-storage devices, as anode material. Again, the unidirectionality of the carrier transport path enhances electron collection. The present endeavor includes such research instances probing towards the amalgamation of these two technologies to indicate the futuristic direction of the self-chargeable storage unit. The present scope is designed broadly in three sections, where the first section deals with the step-by-step improvement of DSSC with a prime focus on the oxide nanotube-based photoanode. The second section deliberates on the research trends for storage devices with the nanotube-based anode. In the last section, the unification of these two technologies within a single chip or area using a common anode is the main emphasis to enhance the utility and green approach for the future world.

Keywords: Energy harnessing, Energy storage, DSSC, Li-ion battery, Na-ion Battery, *In-situ* charging, In-built energy storage.

[*] **Corresponding author Koushik Dutta:** PDPM Indian Institute of Information Technology, Design and Manufacturing, Jabalpur, India; E-mails: koushikdutta@iiitdmj.ac.in, koushikdutta71187@gmail.com

Gopal Rawat & Aniruddh Bahadur Yadav (Eds.)

PREAMBLE

The modern age is going towards automation to facilitate human efforts and vastly dependent on electric power consumption. Electric power generation, conventionally and dominantly, depends on fossil fuel (coal, petroleum, *etc.*), which is not either renewable or everlasting. Additionally, the adverse effect of conventional electric energy generation creates frowning for environmentalists. In this connection, solar power harnessing is the most popular among the ever-present and renewable energy forms, to address the concern. However, the climate condition restricts its continuous generation process, and the spatial distance is the main cause behind storing the energy. Hence, Energy Harvesting devices and Energy Storage devices are inevitable parts of renewable and green energy deployment. For this reason, the amalgamation of these two devices is necessary for a smarter future. Nanotechnological advancement arrowed towards such possibility within a single chip, eventually wearable and flexible form, providing the facility of mobility of the gadgets. In this proposed chapter, the cost-effective way of adjunction of energy harnessing and storage system will be discussed in light of nanostructural evolution for efficient device design with materialistic choice for futuristic applications.

ENERGY HARNESSING IN A COST-EFFECTIVE APPROACH

Restricted source of fossil fuel and their adverse effect through the conventional way of consumption wrinkles the thought process towards sustainable and renewable energy sources. Further, the advancement of nanotechnology thrusts us towards miniaturization and individual deployment of energy requirements. Through the connection, modern research is being focused on the cost-effective approach towards green technologies, which can be reformed towards individual deployment targeting large-scale effects on future generations. For this, solar power generation supported the integrated work with appreciable acceptability among all other renewable energy sources. This section will deal mainly with the cost-effective approach of solar power generation with the evolution strategies adopted by the scientific world.

Introduction

Energy consumption is an inevitable part of human society, and its consumption through different modes (transport, building, and/or individual gadgets) are in increasing pace as the population increases and technologies are invented [1]. In other words, no such fields exist that are powered solely by energy. We are far more reliant on fossil fuels for this purpose [2]. Generally, conventional energy resources, *i.e.*, crude oil and its derivatives, coal-related products, and natural gases, are identified as non-renewable energy sources and are together referred to

as fossil fuels [3]. Compared to renewable energy sources like solar or wind, resources like coal and oil generally give us more energy [4]. According to the statistics, as of May 31, 2022, the total domestic coal output for the years 2021–22 was 137.85 MT, which is a 28.6% increase over the production of 104.83 MT during the same time the previous year [1 - 3]. In Fig. (**1**) the pie chart shows the percentage of generation of electricity by various resources in India in the year 2022 [1 - 3].

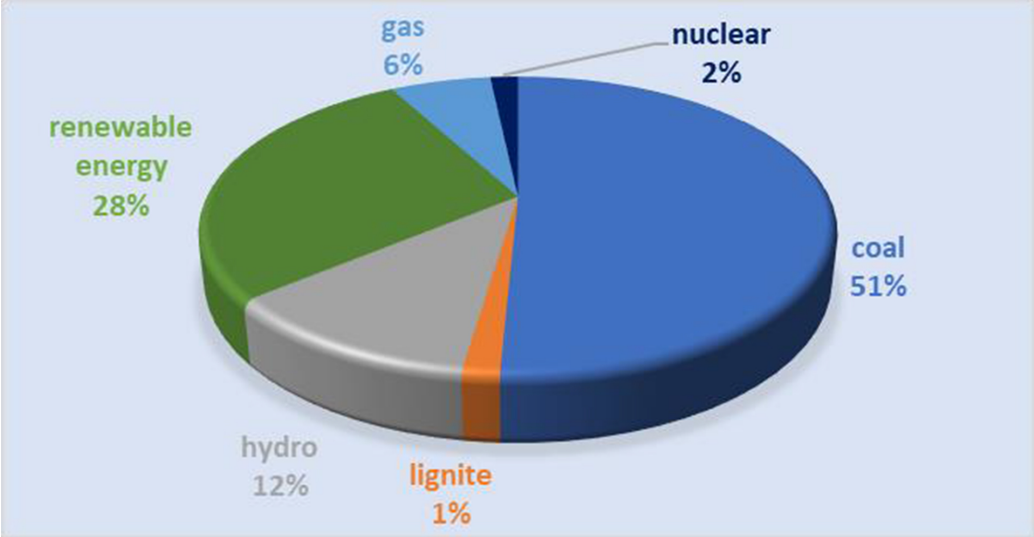


Fig. (1). Sources of electricity in India by installed Capacity 2022.

Non-renewable resources have many drawbacks in addition to their many advantages. The time-consuming nature of non-renewable energy is one of its main drawbacks [1 - 4]. It takes a long time to mine coal, look for oil, install oil drills, construct oil rigs, insert pipes to extract natural gas, and transport it [4, 5]. It also demands great human power as well as cost deployment [5]. As non-renewable energy sources like fossil fuels release chemicals like carbon monoxide, they can be harmful to the environment, and their harsh effects must affect human society in terms of health hazards [5]. A number of health concerns are more likely to affect employees who work in coal mines or oil drilling. As a result, there are numerous illnesses, accidents, and even fatalities [4, 5]. When burned, energy sources like coal, oil, and natural gas generate a lot of carbon dioxide. These substances are contributing to the ozone layer's quick demise. Sulphur oxide and other oxidants generated by the burning of fossil fuels change the precipitation to acid rain [4, 5]. The issues of global warming and climate change are still top-of-mind because fossil fuels emit a lot of greenhouse gases (GHGs), particularly carbon dioxide, into the atmosphere, which has an adverse

SUBJECT INDEX

E

N

O

P

Q

R

S

T

Gopal Rawat

Prof. Gopal Rawat received his M.Tech. and Ph.D. degrees from the Department of Electronics Engineering, IIT (BHU), Varanasi, India with a specialization in microelectronics engineering. After completing Ph.D., he joined as an assistant professor and is currently serving in the School of Computing and Electrical Engineering (SCEE), as a faculty member at IIT Mandi, Himachal Pradesh, India.

Prof. Rawat has a broad research interest in semiconducting materials, micro/nano-electronics, and etc. His research interests include semiconductor devices, circuits, and applications. He has published a number of research articles in leading peer reviewed international journals and conferences such as IEEE Transactions, IEEE Letters, Sensors & Actuators, ACS Applied Electronic Materials, and etc. Besides, he is also involved in book chapters and a few patents. Currently, he is also the principal investigator (PI) of three projects, two of them are Science and Engineering Research Board (SERB) sponsored research projects. Prof. Rawat has also received some prestigious awards and recognition, such as BRICS Young Scientist, etc. He is a senior member of IEEE, USA and lifetime member of Institution of Engineers (India) (IEI). He is also the chapter advisor of IEEE Student Branch at IIT Mandi.

Aniruddh Bahadur Yadav

Prof. Aniruddh Bahadur received Ph.D. degrees from the Department of Electronics Engineering, IIT (BHU), Varanasi, India with a specialization of microelectronics engineering. After completing Ph.D., he joined as a faculty in the Department of Electronics and Communication Engineering Velagapudi Ramakrishna Siddhartha Engineering College Kanuru, Vijayawada, Andhra Pradesh and is currently working as associate professor. Prof. Aniruddh Bahadur Yadav has a broad research interest in semiconducting materials, micro/nano-electronics, one dimensional nanomaterials synthesis by solution route and based sensors for disease diagnosis. He has published 30 plus research articles in leading peer reviewed international journals and conferences such as IEEE Transactions, IEEE Letters, Optical Materials, Journal of Alloys and Compounds, international journal of hydrogen energy and thin solid films etc. He has two book chapters to his credit. He is an editorial member for an IOP publisher journal Materials Research Express. Currently, he is also the principal investigator (PI) of one funded project from BRNS India and completed six medium and short projects under Indian national user program at Indian Institute of Technology Bombay, India.